INICORE
System-on-Chip from Spec to Silicon

Optimized for

Actel CompanionCore

RTCmodule

Description

The RTCmodule is part of Inicore's IPmodule family. The RTCmodule implements the standard functionality of a Real Time Clock. With a synchronous system interface, the module can be integrated in a wide range of systems, from small CPU to a ARM AMBA system.

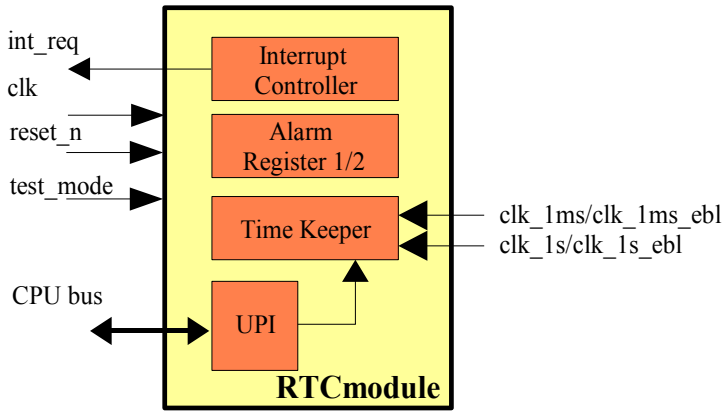

Figure 1: Block diagram

System Bus Interface (UPI): A fully synchronous single clock cycle bus interface provides direct access to all local register resources. See the memory map for detailed description of all registers

Time Keeper: Using either the system clock or an external time reference, the time keeper keeps track of the current time.

Alarm register: Using the alarm register, a preprogrammed system wake-up event can be programmed allowing the CPU to go into a power-down mode.

Interrupt Controller: The interrupt controller bundles all local interrupt sources together and provides one interrupt request line to the main system.

Utilization and Performance Table Optimized for Actel Devices

Family	Device	Utilization				Performance
	- (speed grade)	s-mod	c-mod	RAM	Total	[MHz]
Fusion	AFS250-2	**71**	**686**		12%	**80**
IGLOO	AGL600V5 STD	**72**	**683**		5%	**59**
PA3/E	A3PE600-2	78	751		6%	74
ProASIC^{PLUS}	APA450 STD	73	804		7%	59
Axcelerator	AX250-1	81	435		12%	79
SXA	SX72A-3	83	436		9%	67
eX	EX256	41	72		15%	94

Features

- External or internal reference time
- Counts milliseconds, seconds, minutes and hours of day
- Counts day, month & year
- Automatic end of month and leap recognition
- 2 alarm interrupts
- Seconds, minutes, hour, day, month and year over-roll interrupts
- Time & date are counted in BCD format
- Time is in 24-hour format
- Special test mode to increase test coverage
- Synchronous bus interfaces
  - Zero wait-states
  - Supports system bus such as AMBA APB version 2.0
- Full synchronous design

Applications

- Industrial control
- System-on-Chip
- Peripheral Logic
- Embedded Systems

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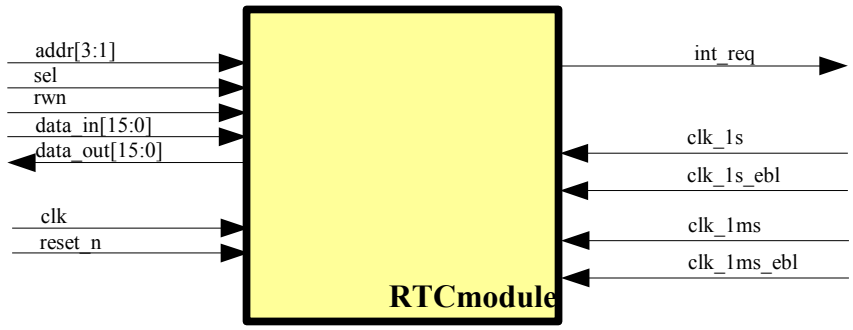

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
Local Bus		
Addr[3:1]	in	Address bus input
data_in[15:0]	in	Data bus input
data_out [15:0]	out	Data bus output
sel	in	Module chip select, active low
rwn	in	Read/write control signal '0': Write '1': Read
int_req	out	Interrupt request, active high
External Reference Clock		
clk_1s	in	1 Hz reference clock
clk_1s_ebl	in	1 Hz reference clock enable
clk_1ms	in	1 KHz reference clock
clk_1ms_ebl	in	1 KHz reference clock enable

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, several configurations are available to optimize the core for the target application:min:

- number of timer alarms
- CPU readback. Configuration value readback can be disabled to minimize gate count.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

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