

iniCAN

Description

The controller area network (CAN) bus, originally developed for the car industry, is a fast, reliable and cost-effective data bus for multi-master and real-time applications. In addition to automotive applications, it is in wide use in applications such as factory automation, machine control, building automation, maritime, medical, railway and avionics. The iniCAN core first was introduced to the market in 1994 and since then is used in a lot of different applications.

The iniCAN core contains all the low-level CAN handling. The user doesn't have to worry about retransmission of an erroneous frame or message arbitration since the CAN framer contains the complete data link layer, including the framer, transmit and receive control, error handling, error reporting and bit synchronization.

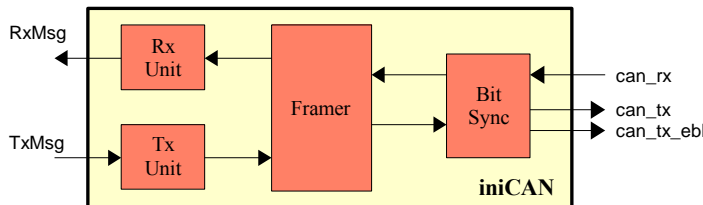


Figure 1: Block diagram

Operation

The core is designed to provide a very simple user interfaces. Sending a message is as simple as setting all control and data bits of the CAN message, set the transmit request line and wait for the acknowledgment on the tx_msg_rdy signal. Receiving a message is not much different: A valid received message is indicated by an active one event on rx_msg_rdy.

Message Filtering

This core doesn't contain any message filters. Acceptance filters are application specific and are designed as add-ons. Inicore provides a wide range of CAN modules that contain the basic CAN framer together with acceptance filters receive and transmit FIFOs, bus coupler and configuration and status registers.

Utilization and Performance Table Optimized for Actel Devices

Family	Device	Utilization			Performance		
		- (speed grade)	s-mod	c-mod	RAM	Total	[MHz]
Fusion							
IGLOO							
PA3/E	A3PE600-2		213	1053		9%	29
ProASIC ^{PLUS}	APA450 STD		212	1257		12%	22
Axcelerator	AX500-3		246	726		12%	40
RTAX	RTAX1000S-1		246	726		5%	24
RTSX	RTSX72S-1		241	786		17%	20

Features

- Full CAN2.0B compliant
- Maximum baudrate 1Mbps
- Achieves 1Mbps with 8MHz system clock
- Built-in CAN error handling
- Access to internal status
- Parallel user side interface for simplifies system embedding
- Local interrupt sources
- Register based design
- Full synchronous design

Applications

- Factory automation
- Machine control
- Automotive
- Avionics and Aerospace
- Building automation

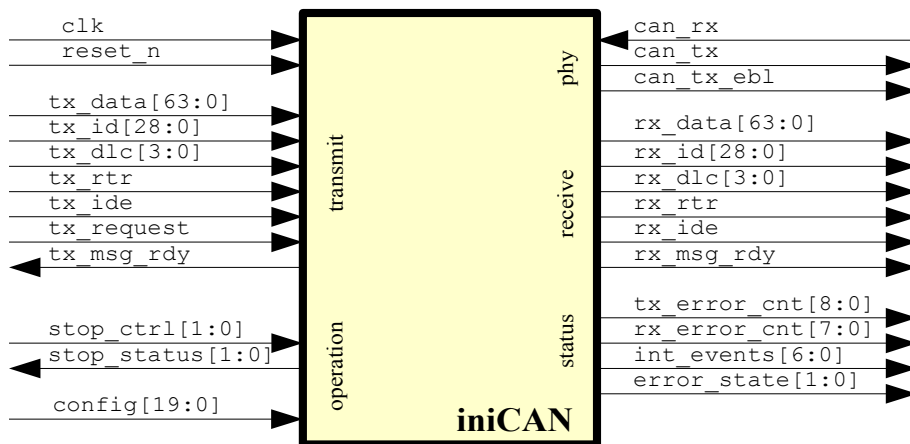


Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
Transmit		
tx_data[63:0]	in	Transmit data
tx_id[28:0]	in	Transmit identified
tx_dlc[3:0]	in	Transmit data length code
tx_rtr	in	Transmit RTR flag
tx_ide	in	Transmit IDE flag
rx_request	in	Transmit request
tx_msg_rdy	out	Transmit message complete
Receive		
rx_data[63:0]	out	Receive data
rx_id[28:0]	out	Receive identified
rx_dlc[3:0]	out	Receive data length code
rx_rtr	out	Receive RTR flag

Pin Name	Type	Description
rx_ide	out	Receive IDE flag
rx_msg_rdy	out	Receive message ready
Operation		
stop_ctrl[1:0]		Stop control
stop_status[1:0]		Stop status
config[19:0]		CAN configuration
Status		
tx_error_cnt[8:0]	out	Transmit error count
rx_error_cnt[7:0]	out	Receive error count
int_events[6:0]	out	Interrupt events
error_state[1:0]	out	CAN controller error state
CANbus		
can_rx	out	CANbus receive signal from external driver
can_tx	in	CANbus transmit signal to external driver
can_tx_ebl	out	CANbus transmit enable for external driver

Implementation

Standard CANbus transceivers can be directly connected to the core. Apart of the receive and transmit data lines, the core provides the transmit data enable to disable the external transceiver when the CAN controller is in bus off error state.

The core is either available in VHDL or Verilog. The design is fully synchronous and can be target to any technology. The RTL source code is accompanied with a self verifying testbench.

About Inicore

- ◆ FPGA and ASIC Design
- ◆ Easy-to-use IP Cores
- ◆ System-on-Chip Solutions
- ◆ Consulting Services
- ◆ ASIC to FPGA Migration
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Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

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