

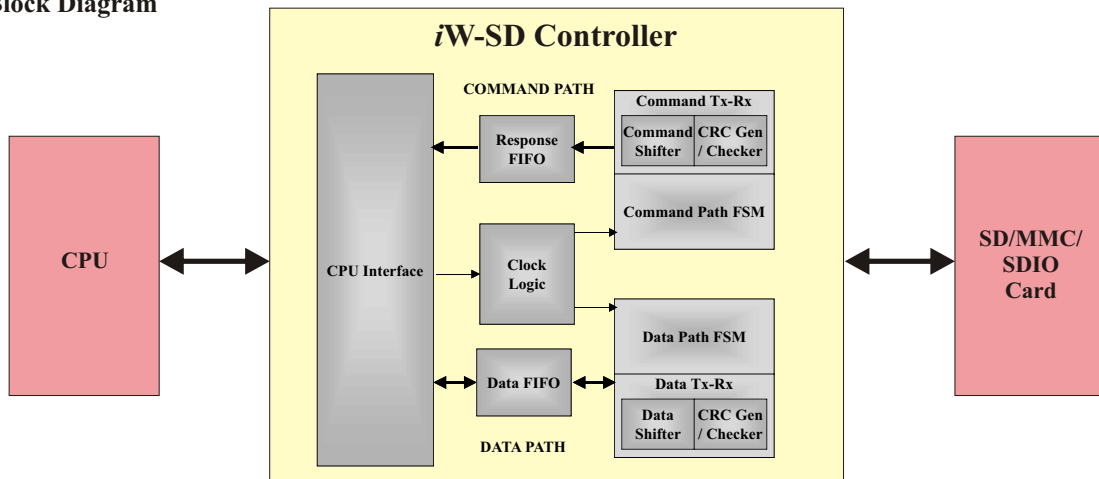
**Overview**

iW-SD Controller interfaces SD / MMC / SDIO card to any processor with a generic interface. The interface towards the SD card is realized by the SD protocol implemented in the controller. The main blocks in the controller are CPU interface, command path state machine, command transmitter/receiver, data path state machine, data transmit/receive and clock logic.

**Features**

- ❖ 1-bit/4-bit modes of SD, MMC and SDIO supported.
- ❖ Supports SPI mode.
- ❖ Both DMA and Interrupt mode is supported for Data transfer.
- ❖ Generic CPU interface.
- ❖ Command buffers to store command index and argument.
- ❖ Any byte size transfers supported. Sector size can be set from 1 byte to 2048 bytes.
- ❖ CRC generation / checking supported for both command and data transactions.
- ❖ Compliant with SDIO specification version 2.0
- ❖ Compliant with SD specification version 2.0
- ❖ Compliant with MMC specification version 2.0
- ❖ Using the SD/SDIO/MMC communication protocol, one SD or SDIO or MMC card is supported.
- ❖ Card Detection / Removal support.
- ❖ Write protect using mechanical switch.
- ❖ Interrupts for errors.

**Block Diagram**



**Device Utilization Summary**

Bus Interface	Actel Family	Device	Tiles	Core Utilization	I/O Cells	RAM Utilization	Frequency	Power
SD2.0/ SDIO2.0/ MMC2.0	ProASIC3	A3P600	3531	25.54%	57	66.67%	50 MHz	193.748 mW
	IGLOO	AGL600	3558	25.74%	57	66.67%	50 MHz	200.312 mW

Note : The above values are for 32-bit generic CPU interface.

**Core Benefits**

- ❖ Eases SOC integration
- ❖ Configurable for ease of use

**Core Application**

- ❖ Used as Host controller for SD, MMC and SDIO cards

**Deliverables**

- ❖ Technical Specification
- ❖ RTL Verilog Synthesizable Code
- ❖ Comprehensive Test Environment
- ❖ Technical Support and Maintenance

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