

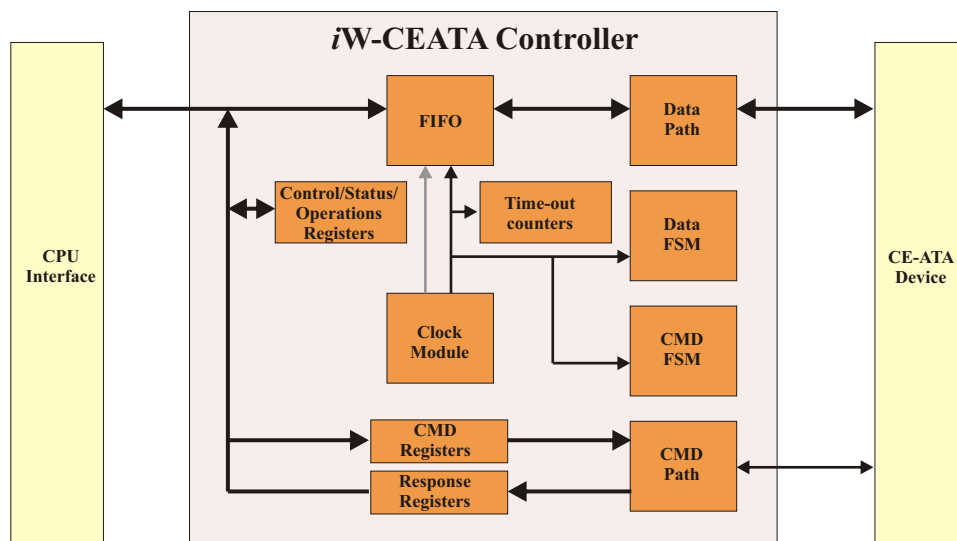
Overview

iW-CEATA Controller is an interface between the processor and the CE-ATA Device. CE-ATA is the interface standard that was derived from MMC with the addition of ATA commands, small form factor, and power-conscious designs used in the latest consumer electronic devices, portable media players, cell phones and other handheld and gaming devices.

Features

- ❖ Compliant to CE-ATA Digital Protocol Revision 1.1
- ❖ Can be used in 1 bit or 4 bit or 8 bit bus width configurations
- ❖ Operates with an input frequency of 50MHz
- ❖ Host clock rate is variable between 200KHz to 50MHz
- ❖ Supports block lengths of 512 bytes, 1Kbytes and 4Kbytes
- ❖ CRC generation / checking supported for both command and data transfer
- ❖ Provides handshake signals during DMA transfers
- ❖ Supports Timeout error indication

Block Diagram



Device Utilization Summary

Bus Interface	Actel Family	Device	Tiles	Core Utilization	I/O cells	RAM Utilization	Frequency	Power
CEATA 1.1	Pro A SIC3	A 3P250	3216	52.34%	62	25%	50 MHz	32.532 mW
	IGLOO	A GL600	3205	23.18%	62	8.33%	50 MHz	32.426 mW

Note : The above values are for 32-bit generic CPU interface.

Core Benefits

- ❖ Eases SOC integration
- ❖ Configurable for ease of use

Core Application

- ❖ Used as Host controller for CE-ATA Device

Deliverables

- ❖ Technical Specification
- ❖ RTL Verilog Synthesizable Code
- ❖ Comprehensive Test Environment
- ❖ Technical Support and Maintenance

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