



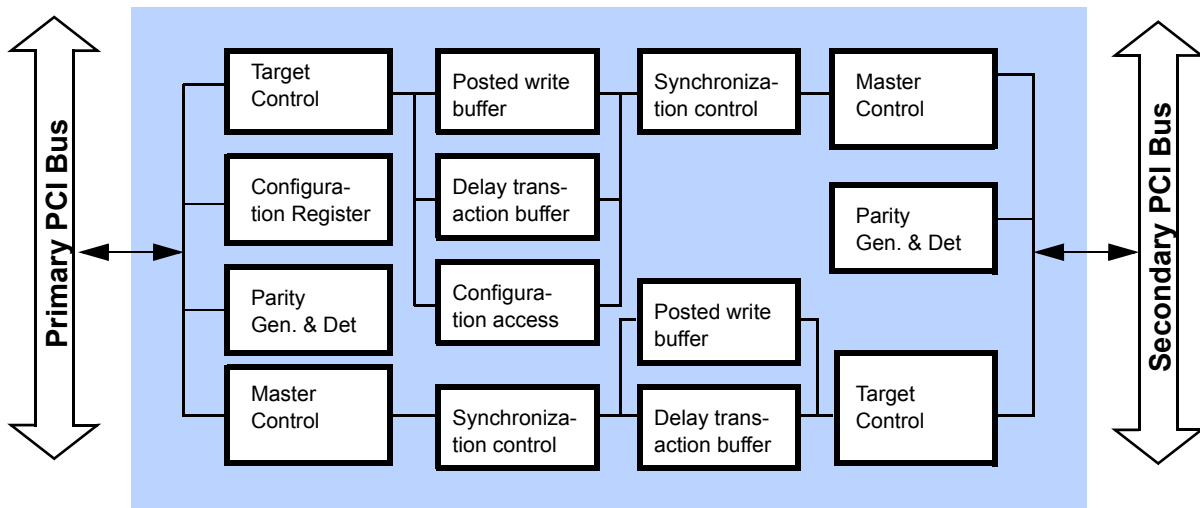
Product Summary

EP440 PCI-to-PCI Bridge

FEATURES

- Fully supports PCI bus specification 2.3 and PCI bridge specification 1.1.
- Independent asynchronous PCI clocks on primary and secondary bus.
- Convert bus transactions between primary bus and secondary bus.
- Combined bus master and target functions on both primary and secondary bus.
 - Master function
 - Initiate PCI memory and IO read/write.
 - Automatic transfer restart on target retry and disconnect.
 - Initiate type 0 and type 1 configuration access on secondary bus.
 - Target function
 - Memory or IO read/write.
 - Receives type 0 and type 1 configuration access on primary bus.
 - Posted memory write transaction and delay transaction on all other transaction types.
- Dual write buffer on each direction supports posted memory write.
- Supports prefetchable and non-prefetchable memory read.
- User specified prefetch limit and write buffer limits.
- Delay transaction processes IO read/write, configuration read/write and memory read transactions.
- Supports target retry, disconnect, master abort and target abort terminations.
- Error reporting and transaction ordering per PCI Bridge specification.
- Includes all PCI-PCI bridge specific configuration registers.

BLOCK DIAGRAM



**DESCRIPTIONS**

The 32-bit PCI-to-PCI bridge is designed for interfacing between the primary PCI bus and the secondary PCI buses. The primary bus is connected to the PCI bus segment that is closer to the host CPU. The secondary bus is connected to the PCI bus segment that is farther away from the host CPU. The EP440 selectively transfer access from the primary PCI bus to the secondary PCI bus and vice versa based on address mapping. The EP440 consists of bus master, bus target, and configuration target functions on the primary side, and it consists of bus master, bus target, and configuration initiation functions on the secondary side.

Immediately after power-up reset, the CPU configures the PCI bridge core by executing configuration access to the bridge. The bridge is detected by the system software just like any PCI devices. The PCI bridge also allows the host CPU to configure all the secondary bus and PCI devices reside on the secondary side the bridge. Type 0 PCI configuration access, if address to the bridge, is processed and responded by the PCI bridge locally. Type 1 PCI configuration, if address to buses and devices located on the secondary side of the bridge, is received by the PCI bridge and forwarded to the secondary bus. If the configuration target resides directly on the secondary bus, the PCI bridge converts the type 1 configuration access to type 0 access so that it can be recognized by PCI devices. It preserves the type 1 access if the target resides behind another bridge device on the secondary bus.

To process normal memory access, the PCI bridge has dual write buffer on each bus interface to post memory write. All memory write and write invalidate data are posted in the write buffers. The transaction is first completed in the originating bus by the PCI bridge as a target of the transaction. The bridge then writes the data from the write buffers to the destination target on the destination bus. The dual write buffer design allows the originating bus to post a second write request to the bridge while the first write request is being processed. The maximum size of each posted write transfer can be defined by the user using the WRITE_LIMIT inputs.

The bridge functions as a bus master on the destination bus. All different types of transfer termination are handled by the core. If a transfer is retried or disconnected by the target in the destination bus, the bridge re-starts the transfer automatically until all posted data are written. Bus request, bus parking, parity detection and generation are all handled by the bridge.

Other than posted memory write, other transaction such as memory read, IO write, configuration access, are processed by the PCI bridge as delay transaction. When the bridge becomes the target of such transaction, it terminates the transfer by using target retry. It then starts the same transaction on the destination bus.

For memory read transactions, the bridge initiate the read access on the destination bus after it is retried on the originating bus. When read data returns from the destination bus, they are stored in the bridge's local read buffer. As soon as the first read data becomes available, subsequent read from the originating bus for the



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same address will be completed normally with data from the read buffer. The bridge may disconnect from the originating master if the master is reading data faster than the rate data is returning from the destination bus.

The bridge distinguishes between prefetchable read data and non-prefetchable read data. Multiple prefetchable data, up to the prefetch boundary, are read at a time unless it is a single read requested by the originating master. Non-prefetchable data are read one data at a time. The PCI bus specification determines when prefetchable or non-prefetchable read should take place. Furthermore, the amount of words to be prefetched can also be determined by user inputs to the bridge by using the PREFETCH_LIMIT input.

I/O read and configuration read access are handled like memory read except that I/O and configuration read is always non-prefetchable.

IO write and configuration write are also handled as delay transaction. They are similar to read access except that data flows in the same direction as the request instead of returning from the destination. The PCI bridge terminates a delayed write normally on the originating bus after it has completed the write transaction on the destination bus.

The PCI bridge processes one delay transaction at a time. It accepts a second delay transaction only after a previous one is completed on the originating bus.

The PCI bridge preserves the transaction orders of all posted and delay transactions as defined by the PCI bridge specification 1.1. It allows posted memory write to pass all delayed transaction while delayed transactions are not allowed to pass posted memory write. This requirement is essential in avoiding deadlock in the bridge between the two buses.

Execution order in both direction of the bridge are general independent of each other. The PCI bridge follows the requirement on the PCI bridge specification 1.1 which requires that before a read transaction can be completed on its originating bus, it must pull out of the bridge any posted write that originated on the opposite side and were posted before the read command completes on the read-destination bus.

OPTIONAL FEATURES

The following table summarizes the optional features which are provided with the PCI bridge as required by user application.

Option	Description
Uni-directional PCI Bridge	Forward request only from primary bus to secondary bus.
Bus arbiter	Arbitration for the primary and/or secondary PCI bus.



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Option	Description
Local PCI slave function	Support multiple base address registers in the primary bus interface to allow other on-chip logic to be mapped to the PCI bus as slave device.
Buffer size	Different buffer size as required by user.

ACTEL DEVICE UTILIZATION DATA

Family	Device (-speed grade)	Utilization			Performance	
		SEQ	COMB	Total	RAM	
ProASIC3	A3PE600-2	2650	5900	65%	18	33Mhz
Axcelerator	AX1000-3	2641	3666	44%	6	33Mhz