DLIN

LIN Bus Controller

ver 1.03

OVERVIEW

The DLIN is soft core of the Local Interconnect Network (LIN) bus controller provides single master with multiple slaves communication concept.

The LIN is a serial communication protocol designed primarity for use in automotive application. Compared to CAN, LIN is a slower but is simplier and more cost efective. It's used in applications where events happen in "human time". It is ideal for communication in intelligent sensors and actuators where the bandwidth and versatility of CAN is not required.

DLIN core provides an interface between a microprocessor/microcontroller and LIN bus. It can work as master or slave LIN node depending on work mode determined by microprocessor/microcontroller. The DLIN controller supports transmission speed between 1kb/s and 20kb/s and can transmit and receive LIN messages compatibible to LIN 1.3 and LIN 2.1. Reported status information includes the type and condition of transfer operations being performed by the DLIN, as well as wide range of LIN error conditions (overrun, framing, parity, timeout). The DLIN includes programmable timer allows detection of timeout and synchronization error. The core is discribed at RTL level allowing target use in FPGA and ASIC technologies.

KEY FEATURES

- Conforms with LIN 2.1 and LIN 1.3 specification
- Automatic LIN Header handling
- Automatic Re-synchronization
- Data rate between 1Kbit/s and 20 Kbit/s
- Master and Slave work modes
- Time-out detection
- Extended error detection
- "Break-in-data" support

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

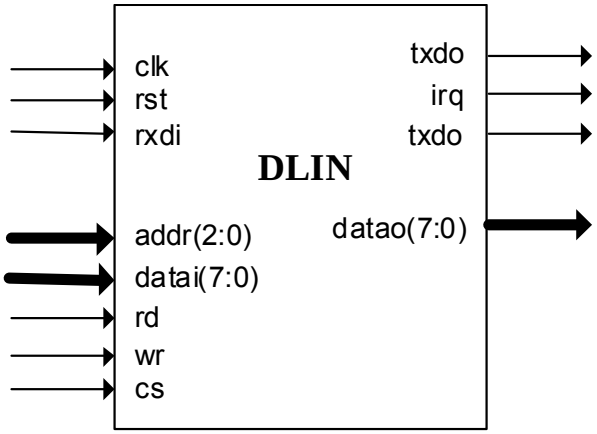
DELIVERABLES

- Source code:
  - VHDL Source Code
  - VERILOG Source Code
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - NCSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts

http://www.DigitalCoreDesign.com
http://www.dcd.pl

- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

SYMBOL

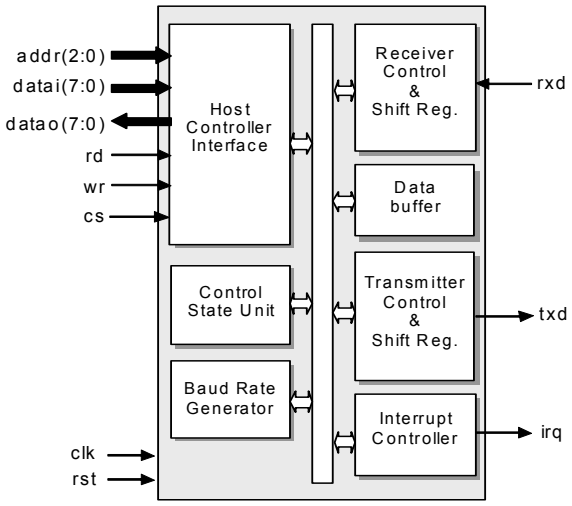


PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
cs	input	Chip select
rd	input	Read data strobe
wr	input	Write data strobe
addr(2:0)	input	Address bus
datai(7:0)	input	Host output data bus
rxd	input	LIN receive data
datao(7:0)	output	Input data bus
irq	output	Interrupt signal
txd	output	LIN transmit data

BLOCK DIAGRAM

Figure below shows the DLIN IP Core block diagram.



Host Controller Interface – accepts inputs from the system bus and generates control signals for other DLIN functionl blocks. Address bus ADDR(2:0) selects one of register to be read from/written into. Active level of RD, WR and CS can be configurable. RD and WR are ignored unless the DLIN has been selected by activing CS input.

Control State Unit– is composed of two state machines, the master and the slave which controls master and slave tasks. The master task handles all bus communication. It must initiate any slave response by sending out a synch break, a synch field and protected identifier field. Slave task is responsible for sending the response message, if is addressed by the master.

Baud Rate Generator – The DLIN contains a programmable 15 bit baud generator which divides clock input by a divisor in the range beteen 1 and (2^{15}-1). The output frequency of the baud generator is 32 x the baud rate. The formula for the divisor is:

$$BR = \frac{f}{(32 \cdot Divisov)}$$

Two registers, called divisor latches DLL and DLH, store the divisor in the 15-bit binary format.

Receiver Control & Shift Register – is responsible for receiving frame from LIN bus.

Provides necessery function for data reception, frame timming and error checking.

Data Buffer – stores the receive or transmit data.

Transmitter Control & Shift Register – Performs transmit management function, sends data by LIN bus

Interrupt Controller – Interrupt controller works with transmitter, receiver and control unit to indicate DLIN transmission events or errors. User can configure which events may generates interrupt by enabled or disabled corresponding bits in Interrupt Enable register. When interrupt was generated host can find information about reason by reading LIN Status Register.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ACTEL® devices after Place & Route (all key features have been included):

Device	Speed grade	Tiles	F_{max}
Axcelerator	-2	1135	107
ProAsic3	-2	1652	102
ProAsic3E	-2	1660	99
Fusion	-2	1660	99

Core performance in ACTEL® devices

CONTACTS

For any modification or special request please contact Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php