D68HC11F

8-bit Microcontroller

ver 1.01

OVERVIEW

Document contains brief description of D68HC11F1 core functionality. The D68HC11F1 is an advanced 8-bit MCU IP Core with highly sophisticated, on-chip peripheral capabilities. The core in standard configuration has integrated on-chip major peripheral functions. An asynchronous serial communications interface (SCI) and separate synchronous serial peripheral interface (SPI) are included. The main 16-bit, free-running timer system has three input capture and five output-compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self-monitoring on-chip circuitry is included to protect D68HC11F1 against system errors. A computer operating properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if illegal opcode is detected.

Two software-controlled power-saving modes, WAIT and STOP, are available to conserve additional power. These modes make the D68HC11F1 IP Core especially attractive for automotive and battery-driven applications.

The D68HC11F1 has built in real time hardware on chip debugger DoCD™, allowing easy software debugging and validation.

D68HC11F1 is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- Software compatible with industry standard 68HC11F1
- Pin-out and memory interface identical to the MC68HC11 Microcontrollers
- Optional enhanced memory interface with De-multiplexed Address/Data Bus to allow easy integration with external memories.
- Interrupt Controller
  - 20 interrupt sources
  - 17 priority levels
- Two power saving modes: STOP, WAI
- Fully synthesizable, static synchronous design with no internal tri-states
- No internal reset generator or gated clock
- Scan test ready

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

http://www.DigitalCoreDesign.com
http://www.dcd.pl

PERIPHERALS

- DoCD™ on Chip Debugger
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
  - Three wire communication interface
- I/O Ports
- Interrupt Controller
  - 20 interrupt sources
  - 17 priority levels
  - Dedicated vector for each interrupt
- Main16-bit timer/counter system
  - 16 bit free running counter
  - Four stage programmable prescaller
  - Real Time Interrupt
- 16-bit Compare/Capture Unit
  - Three input-capture functions
  - Five output-compare channels
  - Events capturing
  - Pulses and digital signals generation
  - Gated timers
  - Sophisticated comparator
  - Pulse width modulation and measuring
- 8-bit Pulse accumulator
  - Two major modes of operation
  - Simple event counter
  - Gated time accumulation
  - Clocked by internal or external source
- SPI –Serial Peripheral Interface M/S
  - Software selectable polarity and phase of serial clock SCK
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
  - Interrupt generation
- Full-duplex UART - SCI
  - Standard Nonreturn to Zero format (NRZ)
  - 8 or 9 bit data transfer
  - Integrated baud rate generator
  - Noise, Overrun and Framing error detection
  - IDLE and BREAK characters generation
  - Wake-up block to recognize UART wake-up from IDLE condition
  - Three SCI related interrupts
- Chip select unit
- ADCCTRL – External ADC converter controller (option)
- EEPROMCTRL – External EEPROM controller (option)

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL simulation macros
  - ModelSim simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
  - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

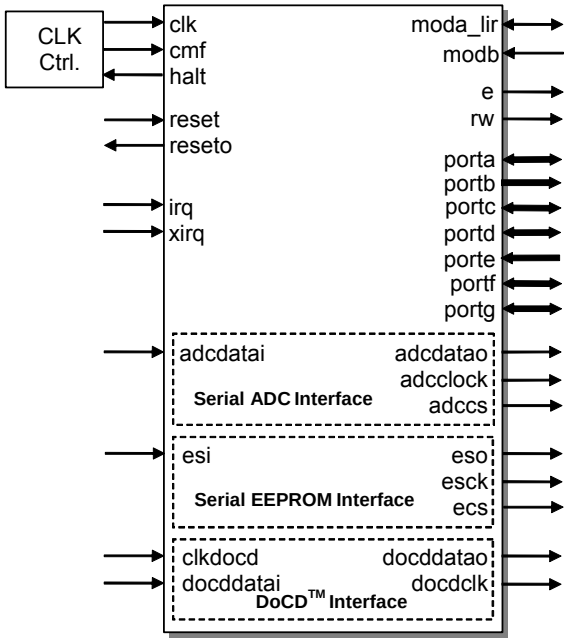
Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL



PINS DESCRIPTION

PIN	ACTIVE	TYPE	DESCRIPTION
clk	-	input	Global system clock
reset	Low	input	Power on reset vector fetch
cmf	Low	input	Clock monitor fail vector fetch
moda_lir	-	inout	Mode A input LIR output
modb	-	input	Mode B input
rw	-	output	RW output
irq	*	input	Interrupt input
xirq	Low	input	Non-maskable interrupt input
e	-	output	Internal E Cycle output
portx	-	inout	Ports I/O pins shared with peripheral functions

D68HC11 Microcontroller pins

adcdatai	-	input	Serial ADC data input
adcdatao	-	output	Serial Data output
adcclock	-	output	Serial Clock to external ADC
adccs	-	output	Chip Select to external ADC

Optional external ADC Controller pins

esi	-	input	Serial EEPROM Data input
eso	-	output	Serial EEPROM Data output
esck	-	output	Serial EEPROM Clock
ecs	-	output	EEPROM Chip Select

Optional external EEPROM controller pins

clkdocd	-	input	DoCD™ clock input
docddatai	-	input	DoCD™ serial Data input
docddatao	-	output	DoCD™ Serial Data Output
docdclk	-	output	DoCD™ Serial Clock Output

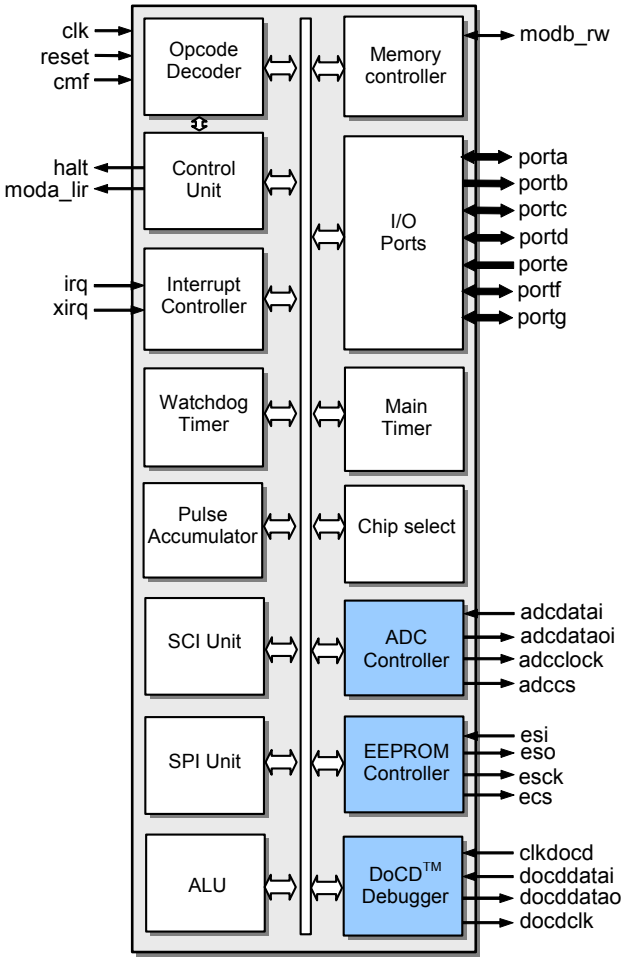
DoCD debugger interface pins

BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and waking-up the processor from the STOP mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks**.**

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index registers X, Y and related logic like arithmetic unit, logic unit, multiplier and divider.



Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface controls access into the program and data memories and special registers. It con-

tains Program Counter (PC), Stack Pointer (SP) register, and related logic.

Interrupt Controller - D68HC11F1 extended IC has implemented 17-level interrupt priority control. The interrupt requests may come from external pins (IRQ and XIRQ) as well as from particular peripherals. The D68HC11F1 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized according to default arrangement established during reset. However any one source may be elevated to the highest maskable priority position using HPRIO register. When interrupt condition occurs, an interrupt status flag is set to indicate the condition.

Timer, Compare Capture & COP Watchdog - This timer system is based on a free-running 16-bit counter with a 4-stage programmable prescaler. A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. Three independent input-capture functions are used to automatically record the time when a selected transition is detected at a respective timer input pin. Five output-compare functions are included for generating output signals or for timing software delays. Since the input-capture and output-compare functions may not be familiar to all users, these concepts are explained in greater detail. A programmable periodic interrupt circuit called RTI is tapped off of the main 16-bit timer counter. Software can select one of four rates for the RTI, which is most commonly used to pace the execution of software routines. The COP watchdog function is loosely related to the main timer in that the clock input to the COP system (clk*2^{17}) is tapped off the free-running counter chain.

The timer subsystem involves more registers and control bits than any other subsystem on the MCU. Each of the three input-capture functions has its own 16-bit time capture latch (input-capture register) and each of the five output-compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI, have their own interrupt controls and separate interrupt vectors. Additional control bits permit software to control the edge(s) that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is essentially a software-oriented system. This structure is easily adaptable to a very wide range of applications although it is not as efficient as dedicated hardware for some specific timing applications.

SCI - The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format : 1 start bit, 8 or 9 data bits and a 1 stop bit. The D68HC11F1 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time, and majority logic decides the sense for the bit. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup) to ignore messages intended for a different receiver. Logic automatically wakes up the receiver in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication that can be used in applications with a modem.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/8. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial periph-

eral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

Pulse Accumulator – This system is based on an 8-bit counter and can be configured to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin present some interesting application possibilities.

I/O Ports - All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD, PORTF, PORTG data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD, DDRF, DDRG to control ports data flow. It assures that all D68HC11F1's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

ADCCTRL – External ADC Controller used as interface between D68HC11F1 internal registers, and external serial/parallel ADC converter. This module has several different options, so its details are described in separate document.

EEPROMCTRL – External Serial EEPROM controller. Manage data exchange between D68HC11F1 and external EEPROM. During initialization copy contents of whole external EEPROM to internal EEPRAM (EEPROM Mirror implemented in standard parallel RAM). This module has several different options, so its details are described in separate document.

DoCD™ - Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

The separate CLKDOCD clock line allow the debugger to operate while the CPU is in STOP mode and the major clock line CLK is stopped.

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented D68HC11 Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- PWM – Pulse Width Modulation Timer/Counter with up to four 8-bit or two 16-bit PWM channels
- I2C Master & Slave bus controllers
  - Master operation
  - Multi-master systems supported
  - Performs arbitration and clock synchronization
  - Interrupt generation
  - Supports speed up to 3,4Mb/s (standard, fast & HS modes)
  - Allows operation from a wide range of clock frequencies (build-in 8-bit timer)
  - User-defined timing
- Floating-Point Arithmetic Coprocessor (DFPAU) IEEE-754 standard single precision
  - FADD, FSUB - addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM - compare
  - FCHS - change sign
  - FABS - absolute value
- Floating-Point Math Coprocessor (DFPMU) - IEEE-754 standard single precision real, word and short integers
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS - change sign
  - FABS - absolute value
  - FSIN, FCOS- sine, cosine
  - FPTAN, FPATAN- tangent, arcs tangent

PERFORMANCE

The following table gives a survey about the Core area and performance in the ACTEL® devices after Place & Route:

Device	Speed grade	Tiles	F_{max}
Axcelerator	-2	5198	39 MHz
ProAsic3	-2	7773	31 MHz
ProAsic3E	-2	7773	30 MHz
Fusion	-2	7725	36 MHz

Core performance in ACTEL® devices

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php

DF68XX FAMILY OVERVIEW

The main features of each DF68XX family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Speed acceleration	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Prg. and Data memories	Compare\Capture	Main Timer System	SCI (UART)	I\O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates
D6802	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	3 900
D6803	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	6 000
D6809	1	64k	64k	-			-	-	-	-	-	-	-	-	-	-	-	✓	9 000
DF6805	4.1	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
D68HC05	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
DF6808	3.2	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
D68HC08	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
D68HC11E	1.0	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓	✓	✓	✓	✓	12 000
D68HC11F	1.0	64K	64K	-	20	17	✓	1*	*	5/3*	1*	✓*	7	✓	✓	✓	✓	✓	13 500
D68HC11KW1	1.0	1M	1M	✓	25	22	✓	1*	*	13/6*	3*	✓*	10	✓	✓	✓	✓	✓	21 000
D68HC11K	1.0	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000
DF6811E	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	12 000
DF6811F	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	13 000
DF6811K	4.4	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000

D68HCXX family of High Performance Microcontroller Cores

\+ optional
* configurable