D16950

Configurable UART with FIFO

ver 1.02

OVERVIEW

The D16950 is a soft core of a Universal Asynchronous Receiver/Transmitter (UART) functionally identical to the OX16C950. The D16950 allows serial transmission in two modes: UART mode and FIFO mode. In FIFO mode internal FIFOs are activated allowing 128 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. The D16950 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). The D16950 includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a n × clock for driving the internal transmitter logic. Provisions are also included to use this n × clock to drive the receiver logic. The D16950 has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

In the FIFO mode, there is a selectable autoflow control feature that can significantly reduce software overload and increase system efficiency by automatically controlling serial data flow through the RTS output and the CTS input signals or by XON and XOFF characters.

The core is perfect for applications, where the UART Core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip, as well as for standalone implementation, where several UARTs are required to be implemented inside a single chip, and driven by some off-chip devices.

The D16950 core includes all 16450, 16550, 16650 and 16750 features and additional functions. The D16950 has ICR registers that gives additional capabilities of configuration of UART work. Data transmission may be synchronize by external clock connected to RI (for receiver and transmitter) or to DSR (only for receiver) pin. NMR register allows to enable 9-bit mode transmission with or without special character. Writing and reading from/to FIFO may be controls by trigger level registers. Trigger level registers may be set any value from 1 to 127.

Two DMA modes are supported: single transfer and multi-transfer. These modes allow UART to interface to higher performance DMA units, which can interleave their transfers between CPU cycles or execute multiple byte transfers.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

KEY FEATURES

- Software compatible with 16450, 16550 , 16750 and 16950 UARTs
- Separate configurable BAUD clock line
- Configuration capability
- Two modes of operation: UART mode and FIFO mode
- Majority Voting Logic
- In the FIFO mode transmitter and receiver are each buffered with 16 / 128 byte FIFO's to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- In UART mode receiver and transmitter are double buffered to eliminate the need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Programmable automatic out-off-band Flow Control logic through Auto-RTS and Auto-CTS
- Programmable automatic Flow Control logic using DTR and DSR
- Programmable automatic in-band Flow Control logic using XON/XOFF characters
- Programmable special characters detection
- Trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-off-band flow control
- RS-485 buffer enable signals
- Transmitter and receiver disable capability
- Fully programmable serial-interface characteristics:
  - *5-, 6-, 7-, 8- or 9-bit characters*
  - *Even, odd, or no-parity bit generation and detection*
  - *1-, 1½-, or 2-stop bit generation*
  - *Baud generation*
  - *Detection of bad data in receiver FIFO*
- Clock prescaler from 1 to 31,875
- Enhanced isochronous clock option
- Complete status reporting capabilities
- False start bit detection
- Line break generation and detection. Internal diagnostic capabilities:
  - *Loop-back controls for communications link fault isolation*
  - *Break, parity, overrun, framing error simulation*
- Full prioritized interrupt system controls
- 9- bit data mode
- Software reset

DESIGN FEATURES

The functionality of the D16950 core is based on the Oxford Semiconductor OX16C950. The following characteristics differentiate the D16950 from Oxford Semiconductor devices:

- The bidirectional data bus has been split onto two separate buses: datai(7:0), datao(7:0)
- The DLL, DLM and THR register are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- RCLK clock source
  - *can be connected to BAUDOUT pin of D16950*
  - *can be clocked externally ,where this clock should be at least two times lower than system clock connected to D16950 CLK pin*
- Fully synthesizable static design with no internal tri-state buffers
- All latches implemented in original 16950 devices are replaced by equivalent flip-flop registers, with the same functionality

APPLICATIONS

- Serial Data communications applications
- Modem interface

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

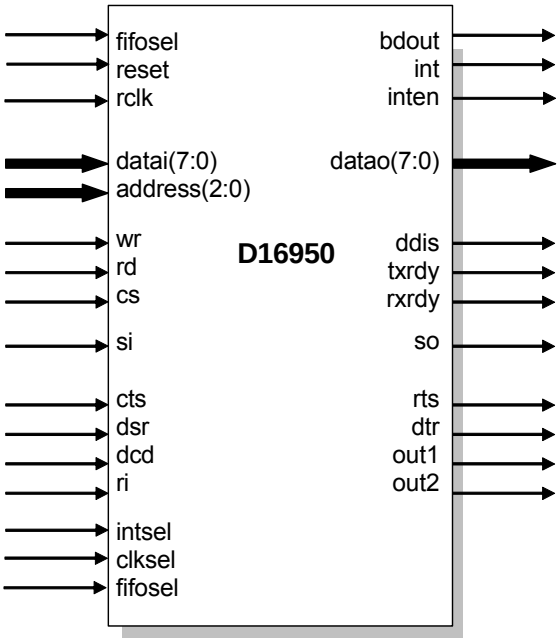
There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

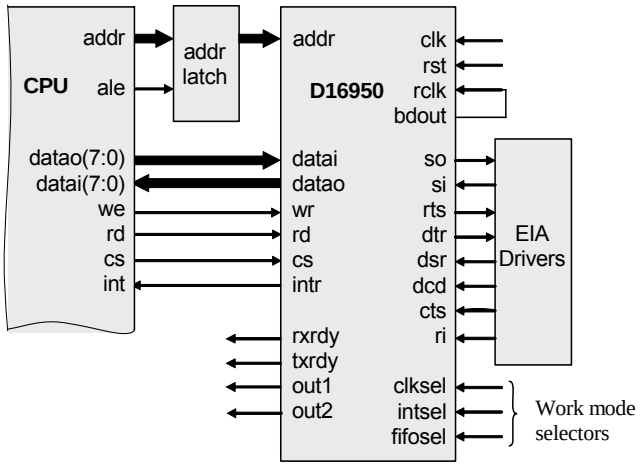
SYMBOL



P INS DESCRIPTION

PIN	TYPE	ACTIVE	DESCRIPTION
reset	input	high	Global reset
clk	input	rising	Global clock
rclk	input	-	Receiver clock
clksel	input	low	Clock prescaler enable
datai	input	-	Parallel data input
addr	input	-	Address bus
wr	input	low	Write input
rd	input	low	Read input
cs	input	low	Chip select input
si	input	-	Serial data input
cts	input	low	Clear to send input
dsr	input	low	Data set ready input
dcd	input	low	Data carrier detect input
ri	input	low	Ring indicator input
fifosel	input	-	Low – enable 16 byte FIFO, high – enable 128 byte FIFO
intsel	input	low	Interrupt select
baudout	output	-	Baud rate output
int	output	high	Interrupt request output
inten	output	high	Enable signal for INT buff.
datao	output	-	Parallel data output
ddis	output	low	Driver disable output
txrdy	output	-	Transmitter ready output
rxrdy	output	-	Receiver ready output
so	output	-	Serial data output
rts	output	low	Request to send output
dtr	output	low	Data terminal ready output
out1	output	low	Output 1
out2	output	low	Output 2

APPLICATION



Typical D16950 and processor connection is shown in figure above.

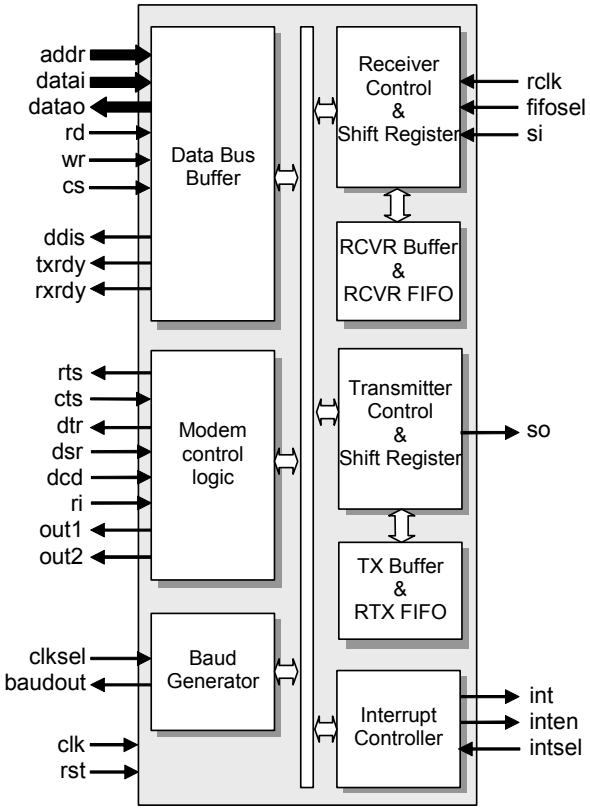
BLOCK DIAGRAM

Data Bus Buffer - The data Bus Buffer accepts inputs from the system bus and generates control signals for the other D16950 functional blocks. Address bus ADDR(2:0) selects one of the register to be read from/written into. Both RD and WE signals are active low, and are qualified by CS; RD and WE are ignored unless the D16950 has been selected by holding CS low.

Baud Generator - The D16950 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range between 1 and (2^{16}–1). Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16950 in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge following the write to DLL or DLM to prevent long counts on initial load. In addition prescaler register is provided which can further divide the clock by values in the range 1,0 to 31,875 in steps of 0,125. Other additional is Time Clock Register (TCR) which allows set the sampling clock between 4 and 16 values. This options of baud rate capable any input clock frequency up to 60MHz.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller - D16950 consists fully prioritized interrupt system controller. It is enabled by INTSEL pin. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Status (ISR) registers.



Receiver Control - Receiving starts when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles as it is shown in figure below. When the logic 1 state is detected during START bit it means that the False Start bit was detected and receiver back to the IDLE state.

Receiver FIFO - The Rx FIFO is 128 levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full, and will not accept any next byte. Any more data entering the Rx shift register will set the Overrun Error flag.

Transmitter Control - module controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter

FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO - the Tx portion of the UART transmits data through SO as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 128 characters (depending on FCR(5) bit value and selected FIFO size). Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx. The UART starts the above operations typically with a Tx interrupt

PERFORMANCE

The following table gives a survey about the Core area and performance in the ACTEL® devices after Place & Route (all key features have been included):

Device	Speed grade	TILES	F_{max}
FUSION[1]	-2	2520	64 MHz
ProASIC3[1]	-2	2520	64 MHz
ProASIC3e[1]	-2	2520	70 MHz
IGLOO[1]	STD	2576	47 MHz
IGLOO+[1]	STD	2576	45 MHz
IGLOOe[1]	STD	2576	40 MHz

[1]- FIFOs implemented in RAM's – 2560 Bits

Core performance in ACTEL® devices

D16X50 UARTS FAMILY OVERVIEW

The family of DCD D16X50 UART IP Cores combine a high–performance, low cost, and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

The D16X50 IP Cores are written in pure VHDL/VERILOG HDL languages which make them technologically independent. All of the D16X50 IP Cores can be fully customized according to customer needs.

Design	UARTS number	UART Mode	FIFO Mode of operation	FIFO Size (Bytes)	Majority voting logic	Separate BAUD Clock line	Software Flow Control	RTS/CTS Flow Control	MODEM Control	False START Bit detection	Complete status reporting	Internal diagnostic capabilities	Prioritized interrupt system	Break generation and detection	IRDA Port	1284 Parallel Port
D16450	1	✓	-	-	✓	✓	-	-	✓	✓	✓	✓	✓	✓	-*	-*
D16550	1	✓	✓	2* 16	✓	✓	-	-	✓	✓	✓	✓	✓	✓	-*	-*
D16750	1	✓	✓	2* 64	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	-*	-*
D16552	2	✓	✓	4* 16	✓	✓	-	-	✓	✓	✓	✓	✓	✓	✓	✓
D16752	2	✓	✓	4* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-*	-*
D16754	4	✓	✓	8* 64	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-*	-*
D16950	1	✓	✓	8* 128	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-*	-*

**-Optional*

D16X50 family of Configurable UARTs with FIFO IP Cores

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