JPEG-E

Baseline JPEG Encoder Core

Implements a high-performance image encoder that complies with the baseline ISO/IEC 10918-1 JPEG standard.

One of the fastest available JPEG cores, the JPEG-E provides a high-performance solution for a variety of image and video compression applications. It can, for example, encode over 30 frames/sec for 4:3 HDTV, 1440x1152, 4:2:0, even in FPGA devices. In a typical 0.18µ process ASIC, the core requires just 62K gates and operates at 320 MHz.

In addition to processing baseline JPEG streams, the core can compress non-standard motion JPEG streams. It can also be enhanced with an optional add-on bit-rate control block, which may benefit applications that have tight bandwidth constraints.

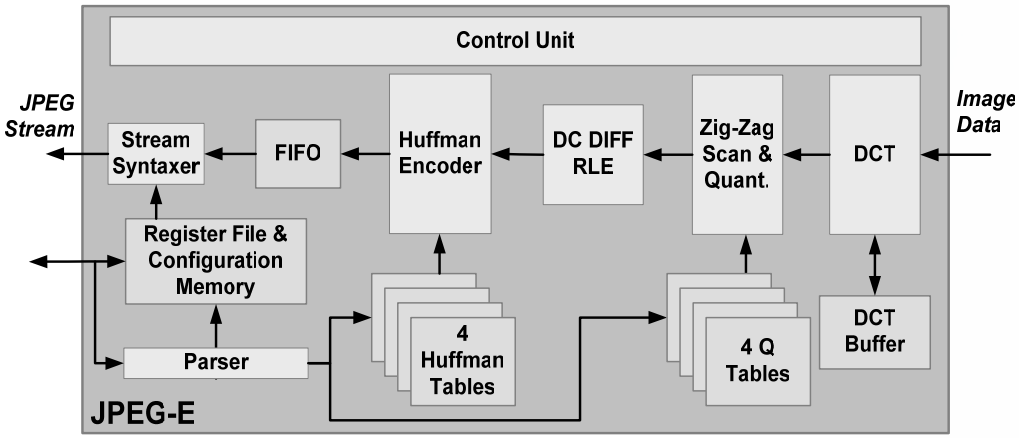
The core includes FIFO-like pixel and stream input/output interfaces. Other standard interfaces (e.g. AMBA) are available. The core is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

Applications

The high-performance JPEG-E core is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

Block Diagram



Features

Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

Additional Image Processing Capabilities

- Motion JPEG encoding/decoding
- Rate Control (optional)

Designed for Easy Integration

- Single clock per input sample for encoding
- Fully programmable through standard JPEG stream marker segments
- Automatic headers generation
- Automatic program-once encode-many operation

Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

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Functional Description

The JPEG-E is configured by feeding it with JPEG headers, which contain table specification, image format, and encoding options data. The core's configuration can be modified after the encoding of one or multiple frames. Image samples in any color space format is input to the JPEG-E in a MCU block by MCU block, raster scan order.

Consuming a single clock cycle per image sample, the JPEG-E can address the most demanding frame-based video compression applications. The JPEG-E outputs a complete JPEG-compliant data stream, including JPEG headers, the size of which can be dynamically controlled if the optional rate-control block is used.

Implementation Results

JPEG-E reference designs have been evaluated in a variety of technologies. The following are sample Actel results optimized for speed.

Actel Device	Cells	Seq	Comb	Frequency	Special Features
Axcelerator AX1000-2	11,943	3,805	8,183	81 MHz	9 RAM
Axcelerator RTAX1000S-1	11,947	3,801	8,146	54 MHz	9 RAM
Proasic Plus APA1000-STD	22,457	3,783	18,674	27 MHz	18 RAM
Proasic3 A3P1000-2	17,214	3,677	13,537	68 MHz	10 RAM

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Actel version includes:

- Post-synthesis EDIF netlist
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)
- Simulation script, vectors, expected results, and comparison utility
- Software (C++) Bit-Accurate Model
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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This core developed by the multimedia experts at Alma Technologies S.A.