

# CAST



## JPEG-D

### Baseline JPEG Decoder Core

#### Features

##### Baseline ISO/IEC 10918-1 JPEG Compliance

- Programmable Huffman Tables (two DC, two AC) and
- Programmable quantization tables (four)
- Up to four color components (optionally extendable to 255 components)
- Supports all possible scan configurations and all JPEG formats for input/output data
- Supports any image size up to 64k x 64k
- Supports DNL and restart markers

##### Additional Image Processing Capabilities

- Motion JPEG decoding
- Decompressing at various resolutions via downscaling in the frequency domain (optional)

##### Designed for Easy Integration

- Stand alone operation
- Automatic self-programming by JPEG stream headers parsing
- Header errors catching
- Broadcasting of decoded image parameters for controlling peripherals such as a raster to block converter

##### Designed for High Quality

- Robust verification environment includes bit-accurate software model
- ASIC and FPGA proven in multiple designs
- Scan-ready design architecture

Implements a high-performance image or video decoder that complies with the baseline ISO/IEC 10918-1 JPEG standard.

One of the fastest available JPEG cores, the JPEG-D provides a high-performance solution for a variety of image and video decompression applications. It can, for example, decode 16:9 HDTV, 1920x1152, 4:2:0, even in FPGA devices. In a typical 0.09 $\mu$  process ASIC, the core requires just 61,000 gates and operates at 450 MHz.

In addition to processing baseline JPEG streams, the core can decompress non-standard motion JPEG streams. It can also be enhanced with an optional IDCT block that enables down-scaling in the frequency domain, a feature that allows decompression at various resolutions from the same compressed stream.

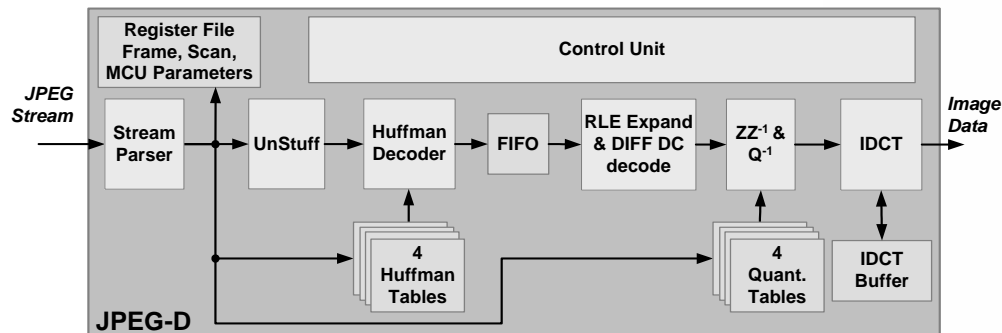
The core includes FIFO-like pixel and stream input/output interfaces, and other standard interfaces (e.g. AMBA) are also available. The core is designed for reliability and ease of integration, and has been proven in a number of ASIC and FPGA designs. The deliverables include a software bit-accurate model that facilitates system on chip verification.

## Applications

The high-performance JPEG-D core is suitable for implementing a variety of multimedia applications, including:

- Digital cameras and camcorders
- Office automation equipment (multifunction printers, scanners, digital copiers etc)
- Medical imaging systems
- Video production suites
- Video conference and display-projection systems
- Surveillance systems

## Block Diagram



## Functional Description

The decoding path is highly autonomous, since the JPEG-D is self-configured (with table, image format and encoding options) by parsing the incoming JPEG stream's headers. The core parses and checks all JPEG marker segments and signals in case it detects an error. Decoded image parameters are made available for controlling peripherals such as a block-to-raster converter.

Designed for continuous data flow, the JPEG-D can address the most demanding frame-based video decompression applications. Optional decoding at various resolutions from the same JPEG data-stream without the need for any extra buffering is enabled when the IDCT block is configured during synthesis to support downscaling in the frequency domain.

## Implementation Results

JPEG-D reference designs have been evaluated in a variety of technologies. The following are sample Actel results.

Actel Device	Cells	Seq	Comb	Frequency	Special Features
Axcelerator AX1000-2	14,609	4,978	9,631	69 MHz	7 RAM
Axcelerator RTAX1000S-1	14,477	5,022	9,455	50 MHz	7 RAM
Proasic Plus APA1000-STD	27,570	5,592	21,978	31 MHz	15 RAM
Proasic3 A3P1000-2	24,293	5,537	18,756	60 MHz	7 RAM

## Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

## Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The Actel version includes:

- Post-synthesis EDIF netlist
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Software (C++) Bit-Accurate Model
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide