Optimized for

UARTmodule

Description

The UARTmodule is part of Inicore's IPmodule family. Universal asynchronous receiver and transmitter using the RS232 protocol are often used to connect peripheral devices to a central controller.

The UARTmodule has one receive and one transmit channel, receive and transmit buffers, an interrupt controller as well as a local bus interface. The built-in receive buffer is configurable in depth, therefore, enabling a gate count and application optimized implementation.

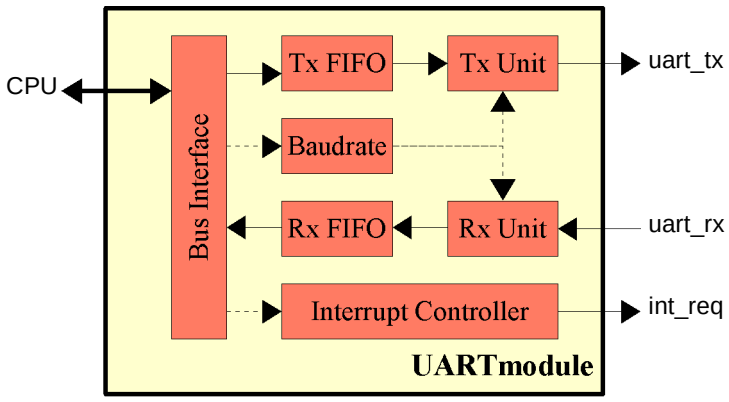

Figure 1: Block diagram

The baudrate generator uses a innovative digital controlled oscillator (DCO) to generate baudrates over a wide frequency range. With a system clock of 8MHz, all baudrates from 1200 baud to 115.2 kbaud have an accuracy of better than 0.1%!

To improve glitch rejection, the receiver uses a 3-point input sampling. Format and parity errors are detected and reported.

Features

- Single channel UART
- Flexible baudrate generator
- Status and error registers
- Scalable RxFIFO (2/4/8/16 bytes deep)
- Double buffered TxFIFO
- 7-bit or 8-bit format
- 1 or 2 stop bits
- Parity enable, even or odd
- Local interrupt controller
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis Options:
  - CPU readback enable
  - CPU bus width
  - RxFIFO depth

Applications

- Industrial control
- System-on-Chip
- Peripheral Logic
- Embedded Systems

Utilization Table Optimized for Actel Devices

Family	Device	Utilization				
	- (speed grade)	s-mod	c-mod	Tiles	RAM	Total
ProASIC[PLUS]	APA150			815		13%
Axcelerator	AX500-3	170	292			6%
SXA	SX32A-3	170	297			16%
eX	EX256	170	297			61%

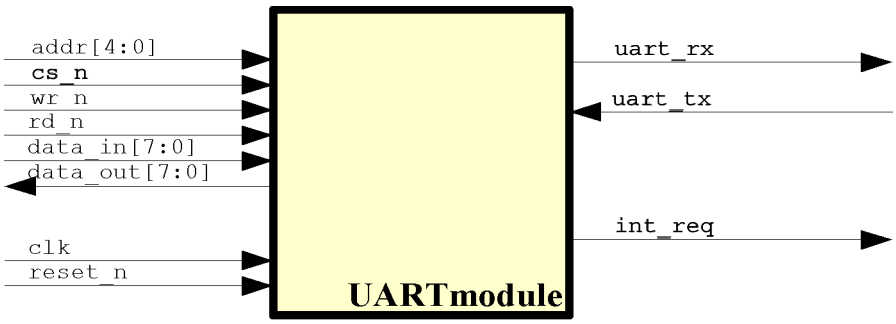

Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[4:0]	in	Address bus input
data_in[7:0]	in	Data bus input
data_out [7:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
int_req	out	Interrupt request
Serial Interface		
uart_tx	out	UART transmit
uart_rx	in	UART receive

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. Synthesis options are included to use the core in 8, 16 or 32-bit systems.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- FPGA and ASIC Design
- Easy-to-use IP Cores
- System-on-Chip Solutions
- Consulting Services
- ASIC to FPGA Migration
- Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Funtional verification testbench
- Synthesis script
- Timing constraints
- User guide

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