
***SmartFusion IEEE 1588 Reference Design
User's Guide***



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Introduction

The SmartFusion™ IEEE 1588 Reference Design demonstrates the use of the Core1588 IP core on a SmartFusion device as part of an IEEE 1588 over Ethernet boundary clock implementation. This reference design is targeted at the SmartFusion Evaluation Board.

The SmartFusion IEEE 1588 Reference Design demonstrates the following Core1588 IP features:

- IEEE 1588 Ethernet packets timestamping
- Synchronization of the precision time clock with a master clock
- Latching of the master synchronized time on input latch assertion
- Triggering output pulses when the synchronized clock reaches specified values

The reference design includes a web server, allowing observation of the current state of the precision time protocol (PTP) clock, and exercises the Core1588 input latches and output triggers.

The SmartFusion IEEE 1588 reference design package contains the following:

- Libero® Integrated Design Environment (IDE) design targeted at the SmartFusion Evaluation Kit hardware. Details about the SmartFusion Evaluation Kit can be found on the SoC Products Group website: http://www.actel.com/products/hardware/devkits_boards/smartfusion_eval.aspx
- SoftConsole, Keil-MDK and IAR Embedded Workbench® projects containing the full source code of the firmware part of the reference design

Programming file of the reference design for the SmartFusion Evaluation Kit
Documentation (this user's guide)

Libero IDE Design

The Libero IDE project implementing the SmartFusion IEEE 1588 reference design is located in the *design_files\Libero_project\IEEE1588_Reference_Design* folder of the reference design package. This Libero IDE project demonstrates the use of Core1588 IP within the SmartFusion FPGA fabric.

Firmware Projects

The firmware projects implementing the firmware part of the IEEE 1588 reference design are located in the *design_files\Firmware\IEEE1588_Reference_Design* folder of the reference design package.

A single folder structure contains the full source code of the firmware and project files for each project:

- SoftConsole
- IAR Embedded Workbench
- Keil-MDK

Programming File

A self contained programming file is provided for use with the SmartFusion Evaluation Kit. This programming file contains both the FPGA fabric design and the firmware executable image. The programming file is located in the *programming_files* folder of the reference design package.

Refer to the "Board Programming" section on page 7 to ensure correct programming of multiple boards.

1 – IEEE 1588 Overview

The IEEE 1588 precision time protocol (PTP) allows synchronization of devices connected to an Ethernet network with a high level of accuracy. One of the devices on the network serves as the master clock. The other devices behave as slave clocks, synchronizing to the master clock's value.

The master clock is dynamically selected among the PTP-capable devices on the network. The IEEE 1588 best master clock (BMC) algorithm is used to determine which device should be used as the master clock device. This algorithm uses the clock's characteristics broadcast on the network through announce messages to determine which clock is the most accurate. Once the BMC algorithm has completed, the master clock starts sending synchronization messages at regular intervals. Slave clocks use these synchronization messages along with communication path delay measurements to adjust their local clock to synchronize with the master clock.

Synchronization to the master is done in two steps:

1. First the communication path's delay is computed by the slave. This is achieved by recording timestamps generated by the Core1588 hardware when IEEE 1588 frames are transmitted or received between the Ethernet MAC and Ethernet PHY.
2. The second step is computing the slave clock offset. This is achieved through the use of timestamps generated when the master clock sends sync frames. Sync frames are sent at one second intervals. These timestamps along with the communication path delay allow computing the offset between the master and slave clock values. This clock offset is used to adjust the slave's clock increment rate to slow down or speed up the slave's clock to converge toward the master clock.

Mean Path Delay Measurement

The mean path delay (Figure 1-1) is measured by initiating a path delay request, then using the timestamp generated as the IEEE 1588 frames of the request and response are transmitted and received. Core1588 generates timestamps when IEEE 1588 frames travel between the Ethernet MAC and Ethernet PHY. These timestamps provide accurate timing of when the various IEEE 1588 frames are sent and received.

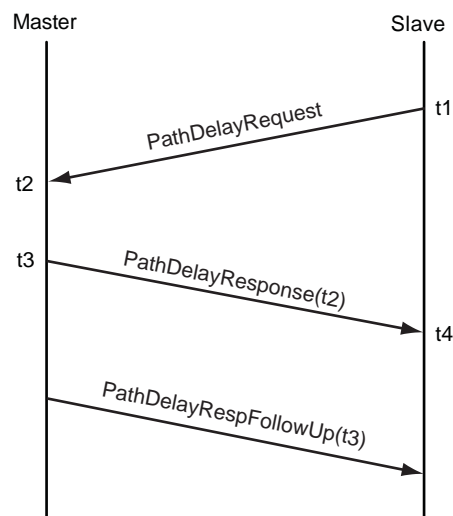


Figure 1-1 • Mean Path Delay

The mean path measurements steps are as follows:

1. The slave initiates the transmission of a path delay request frame.
2. Core1588 captures the time, t_1 , on the slave, at which point the path delay request frame is passed to the Ethernet PHY.
3. Core1588 captures the time, t_2 , on the master, at which point the path delay request frame is received from the Ethernet PHY.
4. The master initiates the transmission of a path delay response frame containing the captured t_2 timestamp.
5. Core1588 captures the time, t_3 , on the master, at which point the path delay response frame is passed to the Ethernet PHY.
6. Core1588 captures the time, t_4 , on the slave, at which point the path delay response frame is received from the PHY.
7. The master transmits a path delay response follow-up frame containing timestamp t_3 .
8. The slave now has timestamps t_1 , t_2 , t_3 , and t_4 .

Assuming that the path delay is fixed and symmetric, we can compute the path delay using [EQ 1-1](#):

$$\text{path_delay} = ((t_2 - t_1) + (t_4 - t_3)) / 2$$

EQ 1-1

Slave Clock Offset Measurement

The slave clock offset measurement is performed at regular intervals as a result of the master sending synchronization frames. The master sends a Sync frame followed by a FollowUp frame every second ([Figure 1-2](#)).

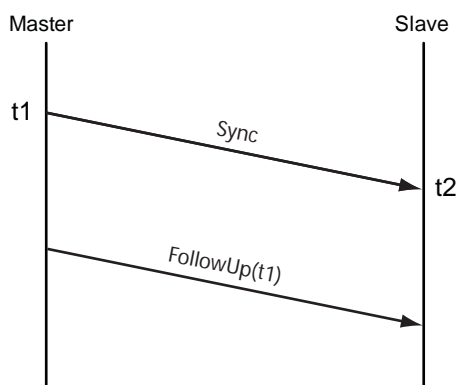


Figure 1-2 • Offset from Master

The slave clock offset measurement steps are as follows:

1. The master initiates the transmission of a sync frame.
2. Core1588 captures the time, t_1 , on the master, at which point the sync frame is passed to the Ethernet PHY.
3. Core1588 captures the time, t_2 , on the slave, at which point the sync frame is received from the Ethernet PHY.
4. The master transmits a follow up frame containing the t_1 timestamp.
5. The slave now has timestamps t_1 and t_2 .

You can compute the slave clock offset using [EQ 1-2](#):

$$\text{slave_clock_offset} = t_2 - t_1 - \text{path_delay}$$

EQ 1-2

2 – Board Programming

This section describes the procedure used for programming the SmartFusion evaluation boards with the IEEE 1588 reference design. Special care is required when programming the boards to ensure that each board is programmed with a unique Ethernet MAC address. The Ethernet MAC address is stored in the SmartFusion MSS eFROM. The eFROM is configured so that the MAC address is incremented as part of the SmartFusion programming through FlashPro.

Note: The lower bits of the Ethernet MAC address are also used as a clock identifier. Failing to follow this programming procedure will result in the clocks not synchronizing with each other because all boards will be using the same clock identifier. All clocks using the same identifier would cause a failure to identify the master clock and the precision time protocol would fail.

Start FlashPro from the Libero IDE project.

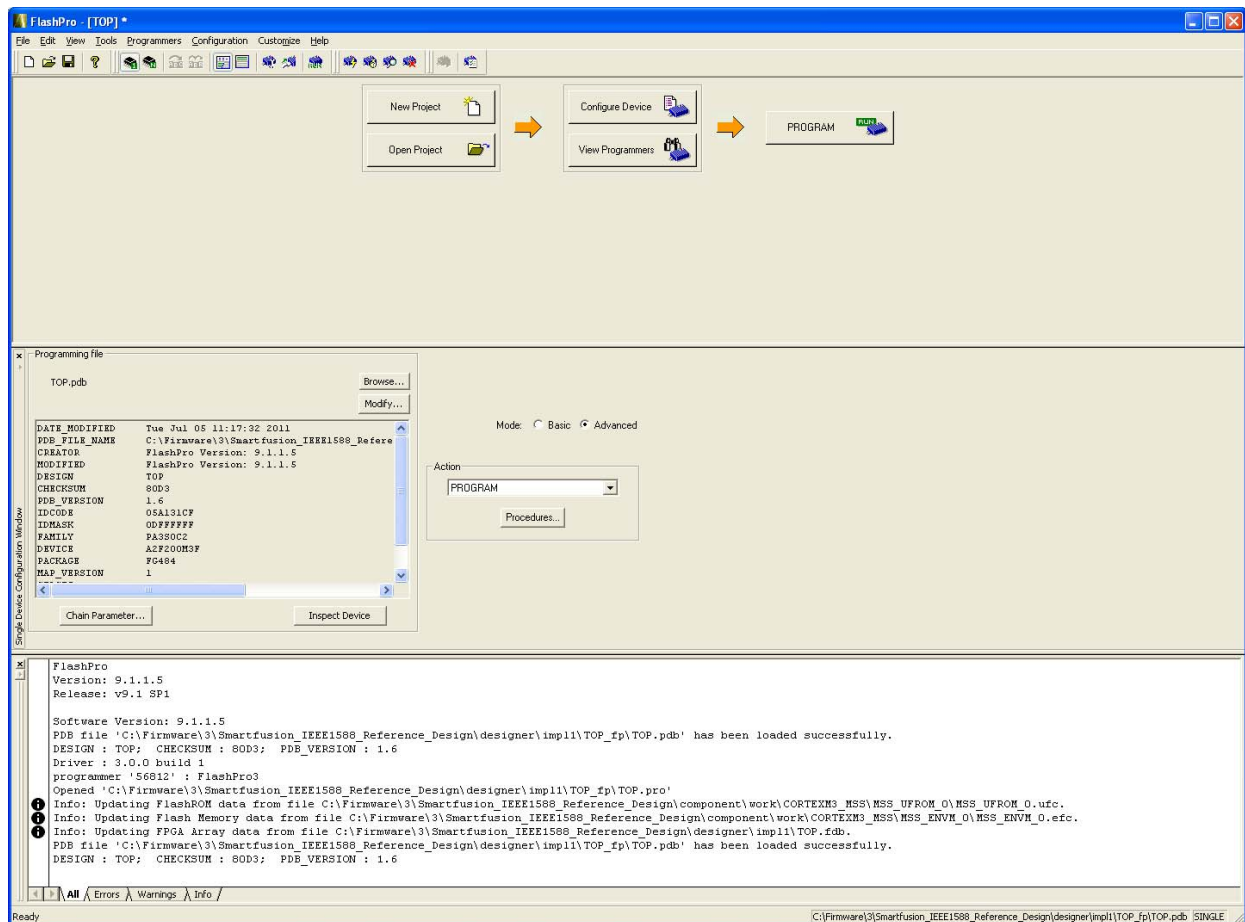


Figure 2-1 • Starting FlashPro from the Libero IDE Project

Click the **Configure Device** button. This will make the Programming file section visible.

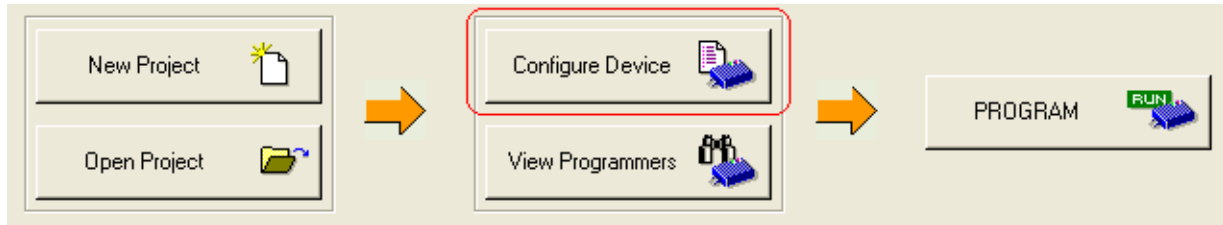


Figure 2-2 • Configure Device Button

Click the **Modify** button. This will open the FlashPoint dialog box.

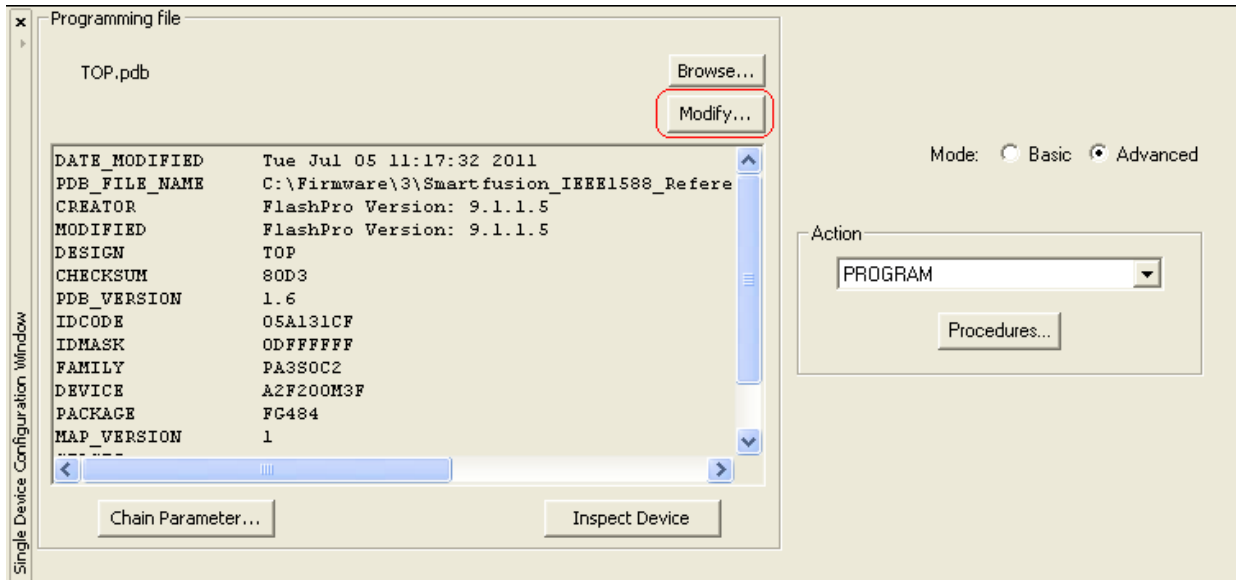


Figure 2-3 • FlashPoint Dialog Box

In the FlashPoint dialog box, click the FlashROM **Modify** button. This will open the Modify FlashROM dialog box.

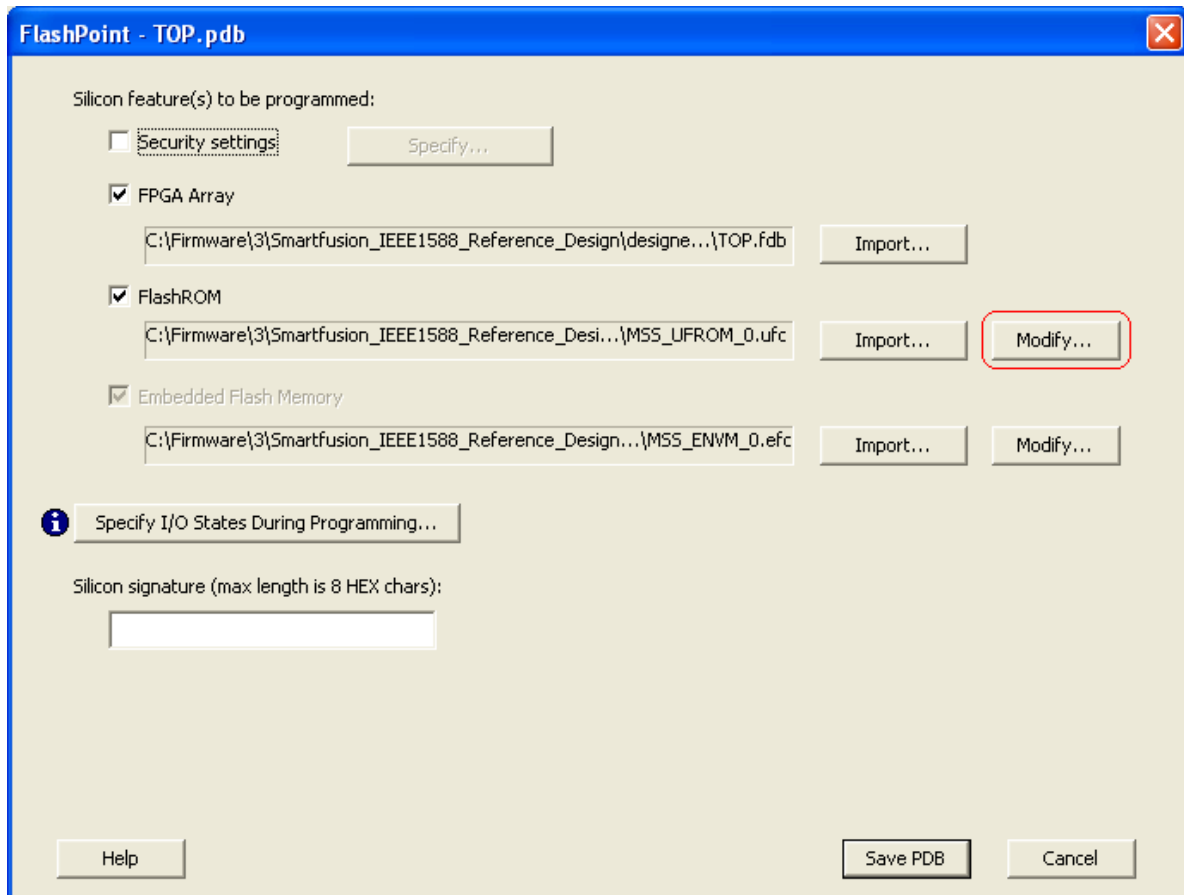


Figure 2-4 • Modify FlashROM Dialog Box

In the Modify FlashROM dialog box, select **Region_0_0** then enter a unique value for **Start value**. This value will be used as the lower bits of the Ethernet MAC address. It will be incremented every time a board is programmed until FlashPro is closed.

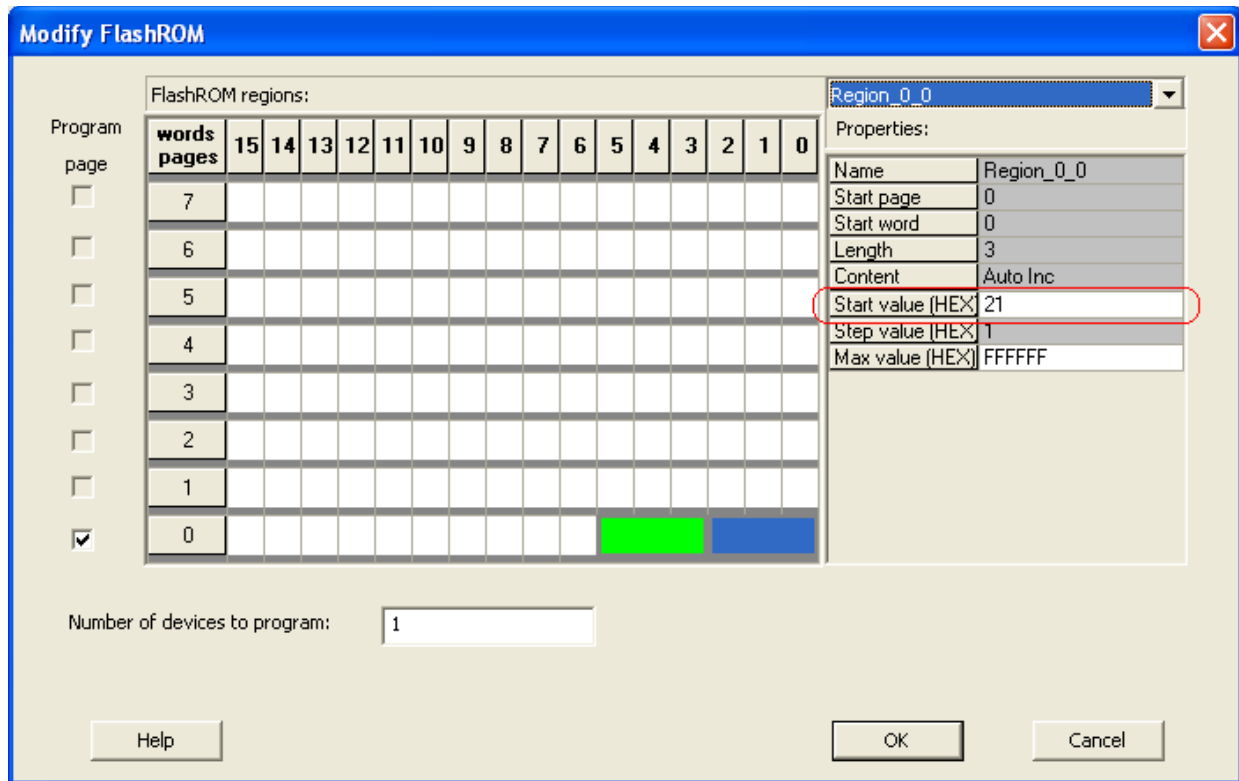
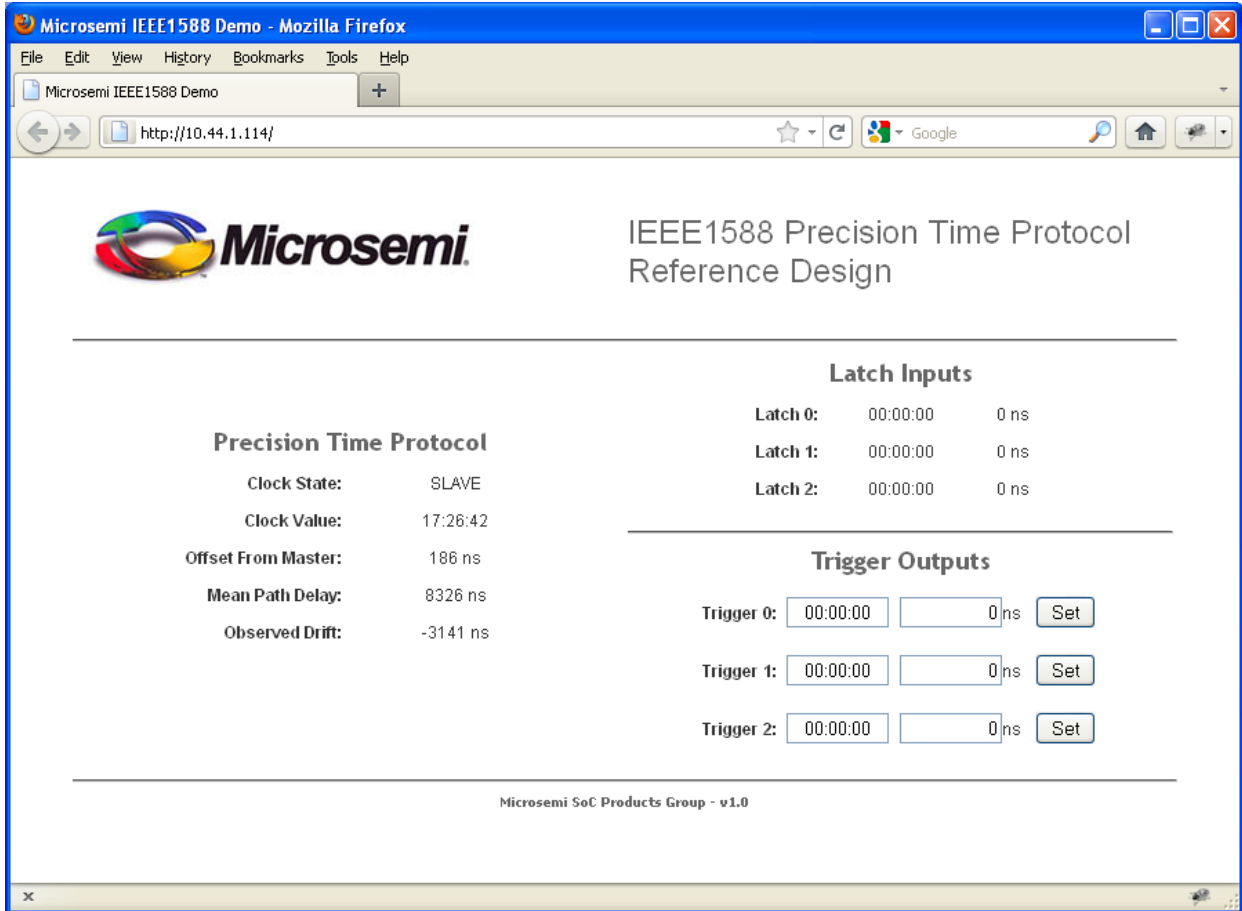


Figure 2-5 • Enter Start Value

You can now click **OK**, **Save PDB** and **Program**. You can program several boards before closing FlashPro.

3 – Web Page Description

The SmartFusion IEEE 1588 Reference Design generates a web page, allowing observation of the state of the precision time protocol clock as well as the Core1588 input latches and output triggers (Figure 3-1).



Precision Time Protocol	
Clock State:	SLAVE
Clock Value:	17:26:42
Offset From Master:	186 ns
Mean Path Delay:	8326 ns
Observed Drift:	-3141 ns

Latch Inputs		
Latch 0:	00:00:00	0 ns
Latch 1:	00:00:00	0 ns
Latch 2:	00:00:00	0 ns

Trigger Outputs		
Trigger 0:	<input type="text" value="00:00:00"/>	<input type="text" value="0 ns"/> <input type="button" value="Set"/>
Trigger 1:	<input type="text" value="00:00:00"/>	<input type="text" value="0 ns"/> <input type="button" value="Set"/>
Trigger 2:	<input type="text" value="00:00:00"/>	<input type="text" value="0 ns"/> <input type="button" value="Set"/>

Microsemi SoC Products Group - v1.0

Figure 3-1 • SmartFusion IEEE 1588 Reference Design Web Page

Accessing the Web Page

The web page generated by the SmartFusion IEEE 1588 Reference Design is accessed by entering the IP address assigned to the SmartFusion evaluation board in the address bar of a web browser. The reference design supports DHCP as the mechanism used to obtain an IP address from the network it is connected to. The IP address is displayed on the first line of the SmartFusion evaluation board's OLED display. IP address 10.44.1.114 was assigned to the board in the example shown in Figure 3-1.

Precision Time Protocol Information

The precision time protocol section of the web page shows the current state of the PTP clock (Figure 3-2).

Precision Time Protocol

Clock State:	SLAVE
Clock Value:	17:26:42
Offset From Master:	186 ns
Mean Path Delay:	8326 ns
Observed Drift:	-3141 ns

Figure 3-2 • Precision Time Protocol Information

Clock State

The Clock State field indicates the current state of the PTP clock. It shows the outcome of the IEEE 1588 best master clock algorithm, indicating whether the local PTP clock is the master clock or a slave clock.

Clock Value

The Clock Value field shows the current value of the PTP clock. The format of the clock value is hours, minutes and seconds as follows: hh:mm:ss.

Nanoseconds are omitted from this field since communication delays between the web browser and board do not allow for an accurate nanoseconds value to be displayed in sync with the actual nanoseconds count on the board.

Offset From Master

The Offset From Master field shows the offset in nanoseconds between the slave and master PTP clocks. It is the measure of how accurately the slave synchronizes to the master clock.

Mean Path Delay

The Mean Path Delay field shows the average time taken by Ethernet frames to travel between master and slave.

Observed Drift

The Observed Drift field shows the measured drift between the slave and master clocks.

Latch Inputs Information

The latch inputs information section of the web page shows the current value of the Core1588 input latches (Figure 3-3).

Latch Inputs

Latch 0:	00:00:00	0 ns
Latch 1:	00:00:00	0 ns
Latch 2:	00:00:00	0 ns

Figure 3-3 • Latch Inputs

The Core1588 input latches take a snapshot of the PTP clock value at the time a Core1588 input latch signal is asserted. This allows accurate timing of system events using FPGA fabric signals. Core1588 includes up to three input latches. Latches 0 and 1 are connected to switches SW1 and SW2 of the SmartFusion evaluation board. Pressing one of these switches will result in display of the PTP clock value in the relevant section of the web page.

Trigger Output Control

The trigger output control section of the web page allows specification of values for the PTP clock at which trigger outputs will become asserted (Figure 3-4).

Trigger Outputs

Trigger 0:	<input type="text" value="00:00:00"/>	<input type="text" value="0"/> ns	<input type="button" value="Set"/>
Trigger 1:	<input type="text" value="00:00:00"/>	<input type="text" value="0"/> ns	<input type="button" value="Set"/>
Trigger 2:	<input type="text" value="00:00:00"/>	<input type="text" value="0"/> ns	<input type="button" value="Set"/>

Figure 3-4 • Trigger Outputs

Core1588 includes up to three trigger outputs, allowing accurate generation of system events through the assertion of FPGA fabric signals. The reference design uses the Core1588 trigger outputs to switch on LEDs 1 to 3 of the SmartFusion evaluation board.

Setting a trigger output time is done by entering the time in hours, minutes, seconds, and nanoseconds, at which the trigger should be asserted and clicking the associated **Set** button.

4 – Software Components Description

The SmartFusion IEEE 1588 Reference Design is built using open source software. The main software components of this reference design areas follows:

- FreeRTOS operating system
- lwIP TCP/IP stack
- PTPd
- Precision time protocol daemon
- Core1588 driver

FreeRTOS

The SmartFusion IEEE 1588 Reference Design uses FreeRTOS version 7.0 as its operating system. The software of the reference design was derived from the Microsemi A2F200M3F Demo project, available from www.freertos.org.

FreeRTOS is licensed under a modified GPL license.

lwIP

The SmartFusion IEEE 1588 Reference Design uses lwIP version 1.4 as its TCP/IP stack. lwIP is licensed under the BSD license. The lwIP TCP/IP stack is available at the following URL:

<http://download.savannah.gnu.org/releases/lwip/lwip-1.4.0.zip>

The http_server example provided as part of the lwIP contributions was used as the starting point of this reference design's web server. The original http_server is available at the following URL:

<http://download.savannah.gnu.org/releases/lwip/contrib-1.4.0.zip>

PTPd

The SmartFusion IEEE 1588 Reference Design uses the PTPd version 2.1.0 precision time protocol daemon to implement the IEEE 1588 protocol. The PTPd source code is freely available under a BSD-style license. PTPd is available from <http://ptpd.sourceforge.net/>.

The original PTPd source code was modified to make use of the Core1588 hardware timestamping capabilities.

Core1588 Driver

The Core1588 driver was developed specifically for this reference design to take advantage of the Core1588's hardware timestamping capabilities.

A – Product Support

Microsemi backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group (formerly Actel) and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650.318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460

800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found on the website at www.actel.com/company/contact/default.aspx.

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