
Accelerator Platform Development Kit

Quickstart Guide



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Introduction

The Axcelerator® Platform Development Kit is a starter kit for working with Actel Axcelerator products and is intended to help you get your Axcelerator product to market faster. The kit consists of a PCI controller board, CorePCIF and CoreSDR design examples, and software drivers to exercise the board. Intended uses are as follows:

- To provide a hardware platform for software driver development specific to your system
- To provide hardware functionality to complement the simulation testbench
- To provide the ability to test modifications and enhancements made to CorePCIF or CoreSDR

Axcelerator Platform Development Kit Documentation

The Axcelerator Platform Development Kit (PFAX DevKit) includes a printed and online version of the *Axcelerator Platform Development Kit Quickstart Guide*, which contains information and procedures for using the PFAX DevKit. The guide is in PDF format on the CD-ROM in the `\doc` directory. To view the online manual, you must have Adobe® Acrobat Reader® installed. Actel provides Acrobat Reader on the Designer CD-ROM.

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Accelerator Platform Development Kit

Overview

The Accelerator Platform (PFAX) Development Kit, as shown in [Figure 1-1](#), contains a 32-bit PCI interface using the Actel CorePCIF IP connected to internal FPGA memory and to external SDRAM memory using the Actel CoreSDRAM IP to control the memory. The included Windows software allows memory tests and DMA transfers to be initiated from the host computer.

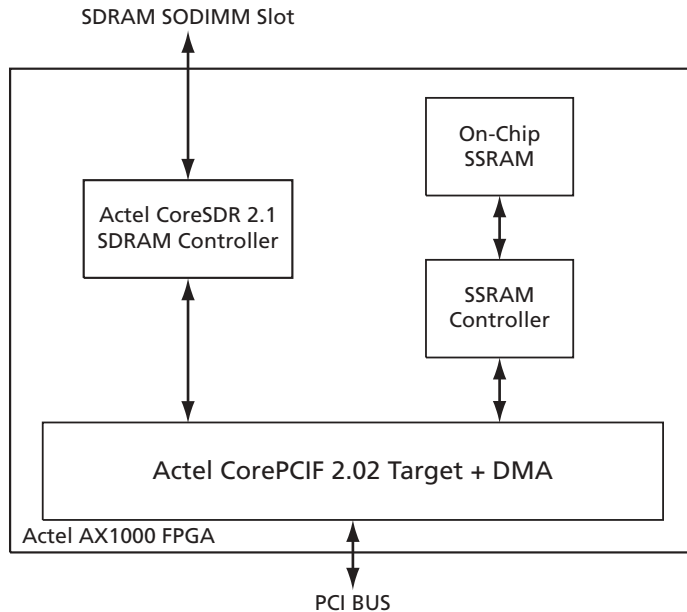


Figure 1-1. Actel Accelerator Platform Development Kit

Development Kit Contents

The following is included with your new Accelerator Platform Development Kit:

Accelerator Platform Board

- PCI card with 64-bit extension (64-bit extension is not used in the current demo)
- Socketed AX1000 device containing the CorePCIF and CoreSDR functions
- Simple, asynchronous backend used to exercise the board
- Header strips for backend observation
- Silicon Explorer connector for viewing internal nodes

CD with Software Drivers and Design Files

- Compiled drivers for either Windows 2000 or Windows XP systems
- Design files for the Actel AX1000 FPGA
- Source code for demo application software (based on the Jungo WinDriver)
- Actel PCI Demo application software
- VHDL source code for the chip-level wrapper (refer to [“Accelerator Platform Development Kit Contents and Uninstall”](#) on page 23 for more information)

Installation

Software Installation

Note: You must install the software before you install the Accelerator Platform Board.

To install the Actel PCI software:

1. Log in as Administrator.
2. Insert the Actel PCI Drivers CD. Installation will start automatically. Follow the instructions on the screen. If installation does not start automatically, run

```
<CDdrive>:\DEMO_software\Setup.EXE
```

Installing the PCI Demo Board

To install the hardware:

1. Turn the computer power off.
2. Install the Axcelerator Platform Development Board using static-safe procedures.
CAUTION: MAKE SURE THE SDRAM SODIMM IS NOT POPULATED ON THE AXCELERATOR PLATFORM BOARD IN A 5-VOLT SYSTEM.
3. Boot your PC and log in as Administrator if required. When the New Hardware Wizard appears, click **Next** and then select **Display list of the known drivers**. Click **Next** again.
4. Select **Show compatible hardware drivers**.
5. Select **Actel Axcelerator Platform Development Board**. Click **Next**, then **Next** again.
6. Click **Finish**. Installation is now complete.

Refer to [“Axcelerator Platform Development Kit Contents and Uninstall”](#) on page 23 for instructions on how to remove the PCI card.

Using the Platform Board

With the Axcelerator Platform Development Board, Actel supplies a basic Windows utility that enables you to peek, poke, fill, and display the PCI/RT memory.

Exercising the PFAI Demo Board

This development kit provides you a demo application to exercise basic PCI access to the SDRAM. The demo application allows basic reads and writes to the SSRAM.

Running the Demo Software

To execute the demo application, select the Actel PCI program from the **Start** menu (from the **Start** menu, select **Programs > Actel PCI > Actel PCI**).

Demo Application Window

The Operations Panel of the demo application is shown in [Figure 2-1](#).

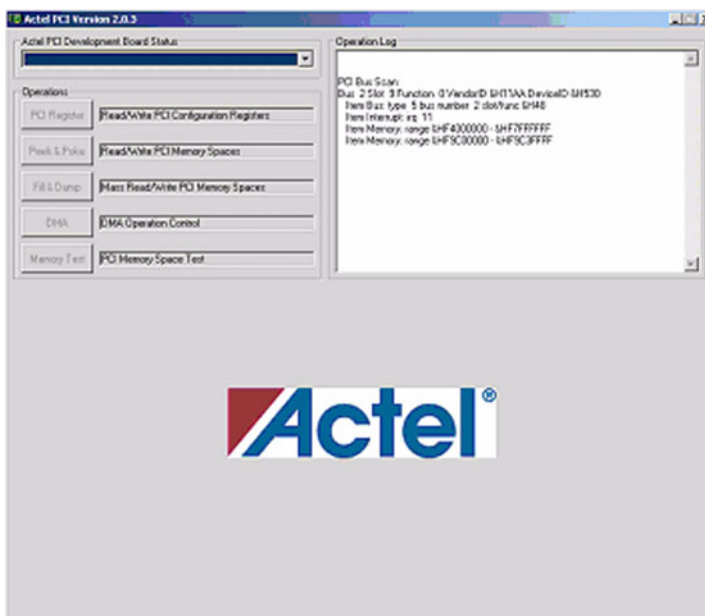


Figure 2-1. Demo Application Window

Select PCI Card

Select the target PCI card from the dropdown list Actel PCI Development Board Status (Figure 2-2).

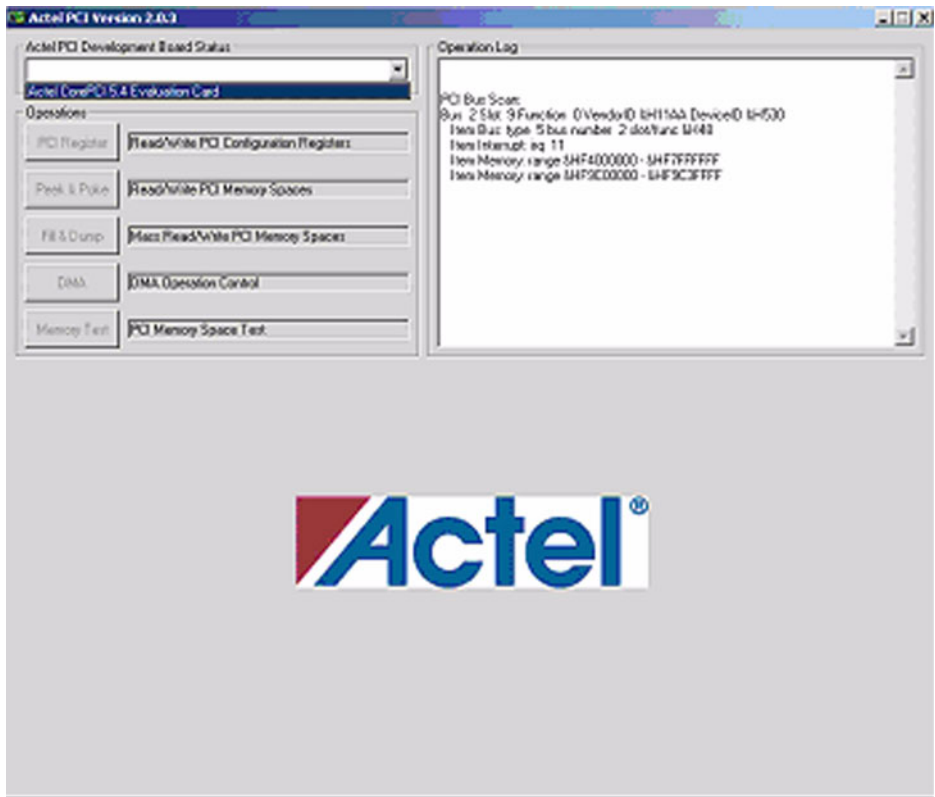


Figure 2-2. Select Target PCI Card

PCI Configuration Space

To access the PCI configuration space, click the **PCI Register** button in the Operations Panel (Figure 2-1 on page 11). The PCI Configuration Register Panel appears, as shown in Figure 2-3.

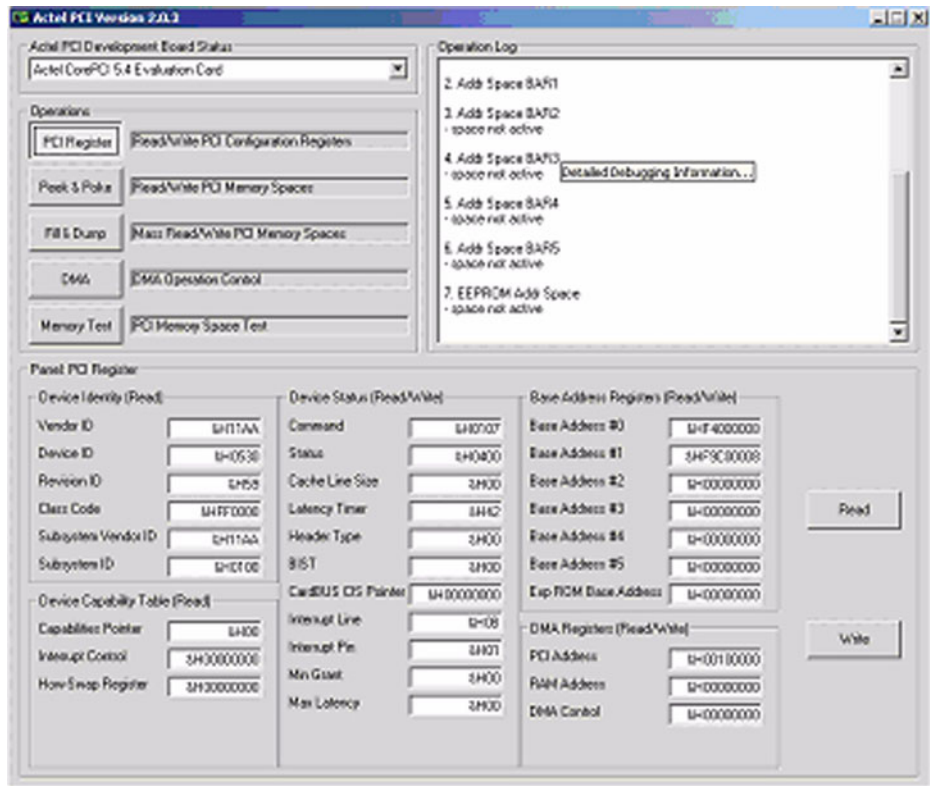


Figure 2-3. PCI Configuration Register Panel

Memory Test

Click the **Memory Test** button in the Operations Panel (Figure 2-1 on page 11) to perform a memory test. The Memory Test Panel appears, as shown in Figure 2-4.

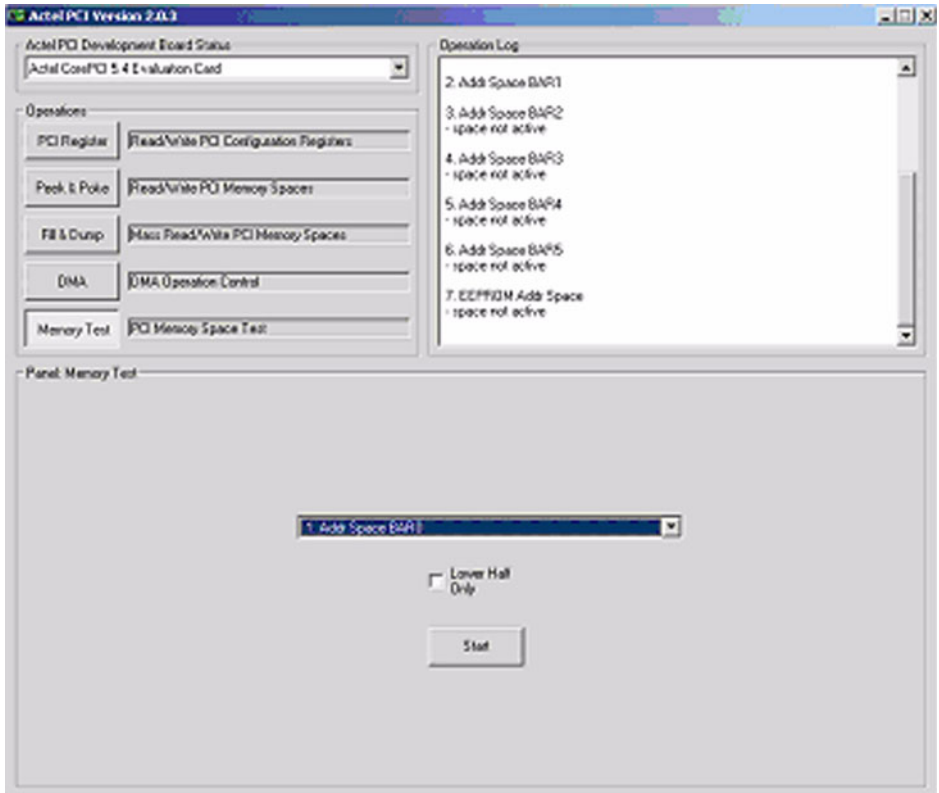


Figure 2-4. Memory Test Panel

Peek and Poke

To read or write a specific value to a specific location in memory, click the **Peek & Poke** button on the Operations Panel (Figure 2-1 on page 11). The Peek & Poke Panel appears, as shown in Figure 2-5.

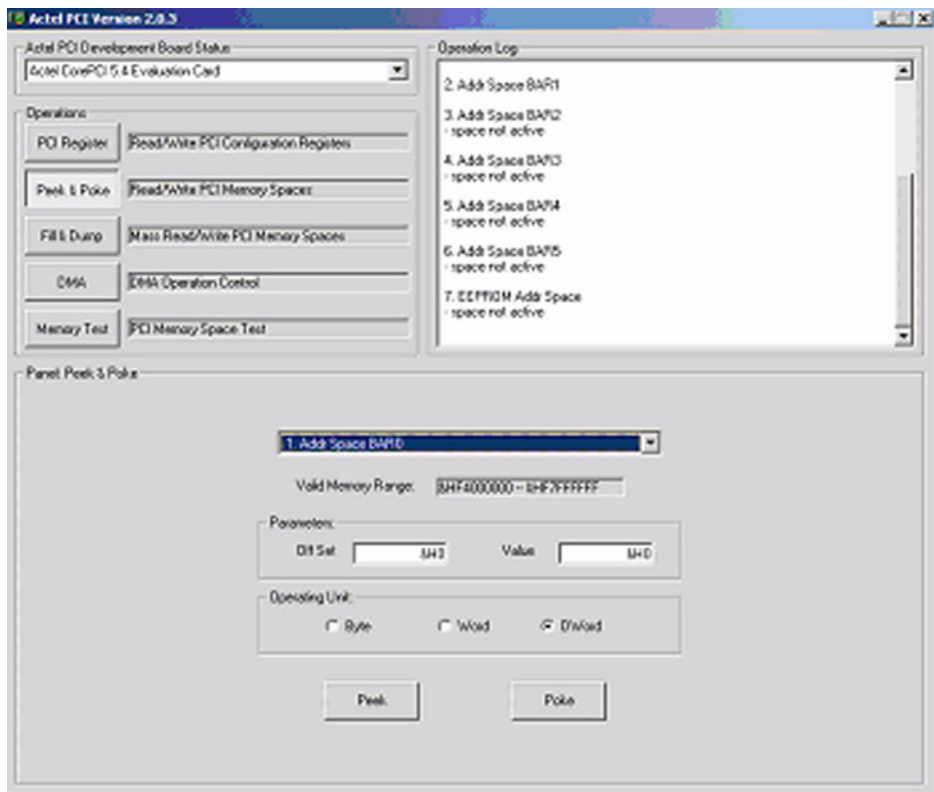


Figure 2-5. Peek & Poke Panel

Provide the parameters and operation unit, then click the **Peek** button to perform a memory read or the **Poke** button to perform a memory write.

Fill and Dump

To read or write values to consecutive memory locations, click the **Fill & Dump** button in the Operations Panel (Figure 2-1 on page 11). The Fill & Dump Panel appears, as shown in Figure 2-6.

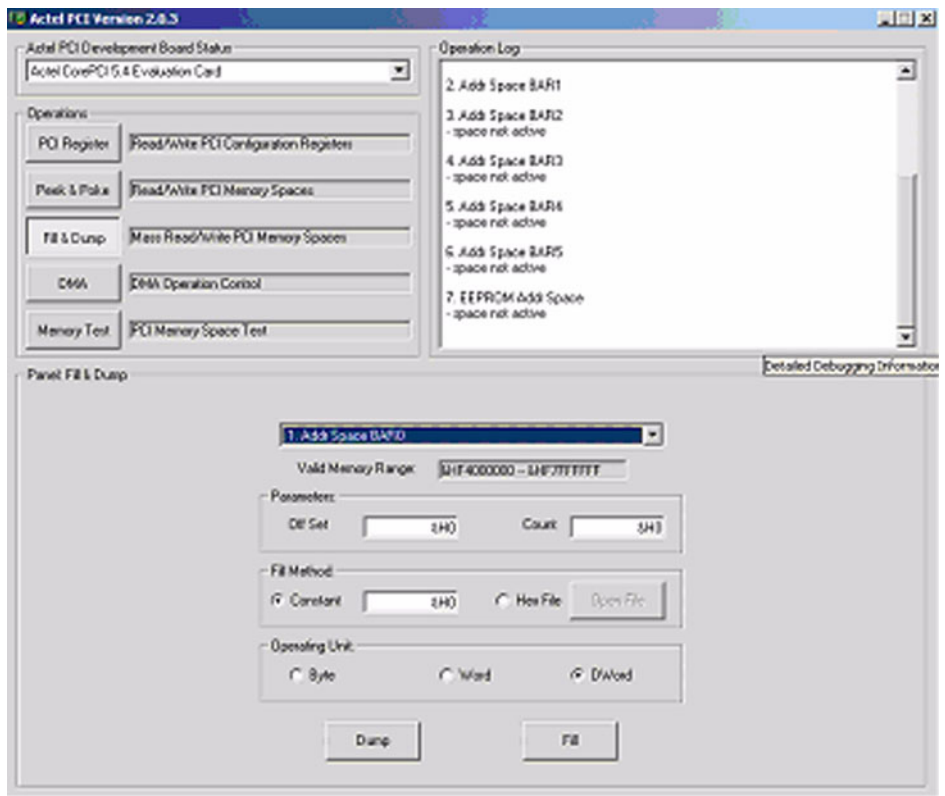


Figure 2-6. Fill & Dump Panel

Provide the parameters, operation method, and operation unit, then click the **Dump** button to perform a memory dump or the **Fill** button to perform a memory fill.

Software Driver/Application Development

The Axcelerator Platform Demo Board conforms to the configuration space mapping defined in the *CorePCIF datasheet* on the Actel website. You can use the hardware to test your own drivers and applications developed from scratch or from the sample code provided in the kit. The sample code provided in the kit is based on the Jungo WinDriver development kit. Refer to “[Axcelerator Platform Development Kit Contents and Uninstall](#)” on page 23 for the location of the sample code in the kit. To obtain the WinDriver development kit, contact Jungo Systems at <http://www.jungo.com>.

Hardware Prototyping

The PFAX DevKit can also be used to test modifications made to the core or custom backends using a daughter board strategy. In either case, a new device can be programmed and inserted into the socket.

Board Description

The Axcelerator Platform Board is illustrated in [Figure 3-1 on page 18](#). The main components on the board are the socketed FPGA, the Silicon Explorer connector, the backend header strips, the RS-232 transceiver, and the SDRAM SODIMM interface. The RS-232 interface is not used in the current design. The board includes the 64-bit PCI extension; however, the extension is not used.

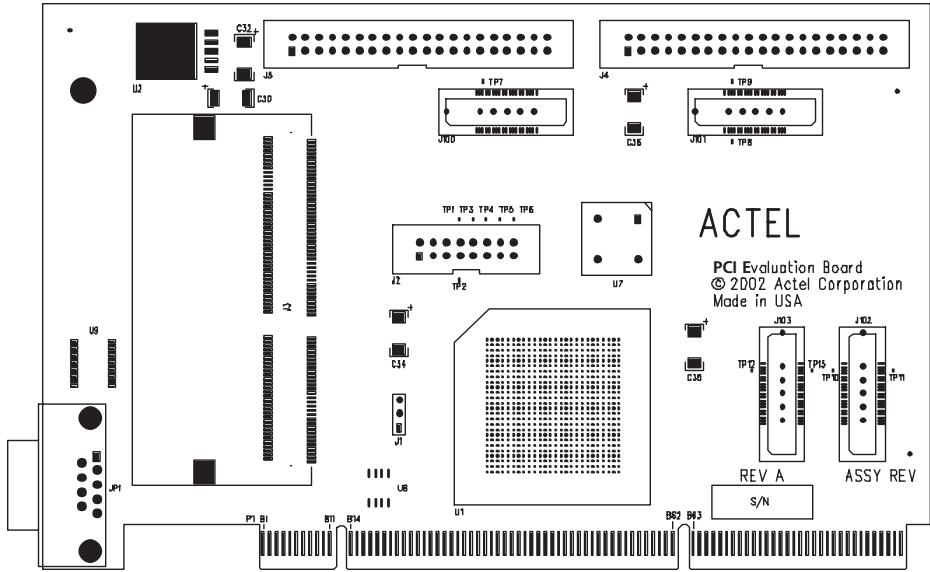


Figure 3-1. Axcelerator Platform Board

Table 3-1 describes the PCI demo board components.

Table 3-1. Axcelerator Platform Board Legend

Reference Designator	Description
J1	General Purpose Test Header
J2	General Purpose Test Header
J3	Mictor Logic Analyzer Header (Not Fitted)
J4	Mictor Logic Analyzer Header (Not Fitted)
J5	Silicon Explorer Connection
J6	Mictor Logic Analyzer Header (Not Fitted)
J7	Mictor Logic Analyzer Header (Not Fitted)
J9	SDRAM SODIMM Interface
JP1	RS-232 Transceiver
U3	Actel AX1000 FPGA

Signals and Connections

Table 3-2 to Table 3-4 on page 21 provide connection information for the FPGA, the PCI bus, and the general purpose test header strips.

Table 3-2. PCI Signal Connection Table

PCI Signal	AX1000 Pin Number	PCI Signal	AX1000 Pin Number
CLK	B12	AD23	AF3
RST	AE15	AD24	AC2
AD0	AA12	AD25	AB3
AD1	AB12	AD26	AB2
AD2	AC12	AD27	AA3
AD3	Y11	AD28	AA2
AD4	AC11	AD29	AA1
AD5	AA10	AD30	Y3
AD6	AB10	AD31	Y2
AD7	AC10	CBE0	AE10
AD8	AF10	CBE1	AB7
AD9	AC9	CBE2	AC5
AD10	AD9	CBE3	AC3
AD11	AE9	DEVSELN	AC6
AD12	AF9	FRAMEN	AF6
AD13	AC8	GNTN	W3
AD14	AD8	IDSEL	AD2
AD15	AE8	INTAN	W2
AD16	AD5	IRDYN	AE6
AD17	AE5	PAR	AC7
AD18	AF5	PERRN	AE7
AD19	AD4	REQN	Y1
AD20	AE4	SERRN	AD7
AD21	AF4	STOPN	AB6
AD22	AE3	TRDYN	AD6

Table 3-3. Header Strip J1

Header Pin	Signal	FPGA Pin	Header Pin	Signal	FPGA Pin
1	GND	N/A	2	GND	N/A
3	5.0 V	N/A	4	3.3 V	N/A
5	POD_A_ODD15	E17	6	POD_A_EVEN15	E11
7	POD_A_ODD14	F17	8	POD_A_EVEN14	F11
9	POD_A_ODD13	A18	10	POD_A_EVEN13	G11
11	POD_A_ODD12	B18	12	POD_A_EVEN12	C12
13	POD_A_ODD11	C18	14	POD_A_EVEN11	F12
15	POD_A_ODD10	B19	16	POD_A_EVEN10	G12
17	POD_A_ODD9	C19	18	POD_A_EVEN9	F15
19	POD_A_ODD8	D19	20	POD_A_EVEN8	G15
21	POD_A_ODD7	E19	22	POD_A_EVEN7	A16
23	POD_A_ODD6	F19	24	POD_A_EVEN6	B16
25	POD_A_ODD5	A20	26	POD_A_EVEN5	D16
27	POD_A_ODD4	B20	28	POD_A_EVEN4	E16
29	POD_A_ODD3	C20	30	POD_A_EVEN3	F16
31	POD_A_ODD2	D20	32	POD_A_EVEN2	G16
33	POD_A_ODD1	E20	34	POD_A_EVEN1	A17
35	POD_A_ODD0	B21	36	POD_A_EVEN0	C17
37	3.3 V	N/A	38	5.0 V	N/A
39	GND	N/A	40	GND	N/A

Table 3-4. Header Strip J2

Header Pin	Signal	FPGA Pin	Header Pin	Signal	FPGA Pin
1	GND	N/A	2	GND	N/A
3	5.0 V	N/A	4	3.3 V	N/A
5	POD_B_ODD15	G25	6	POD_B_EVEN15	C21
7	POD_B_ODD14	G24	8	POD_B_EVEN14	D21
9	POD_B_ODD13	G23	10	POD_B_EVEN13	E21
11	POD_B_ODD12	H25	12	POD_B_EVEN12	B22
13	POD_B_ODD11	H24	14	POD_B_EVEN11	C22
15	POD_B_ODD10	J26	16	POD_B_EVEN10	D22
17	POD_B_ODD9	J25	18	POD_B_EVEN9	A23
19	POD_B_ODD8	J24	20	POD_B_EVEN8	B23
21	POD_B_ODD7	J23	22	POD_B_EVEN7	C23
23	POD_B_ODD6	J22	24	POD_B_EVEN6	D23
25	POD_B_ODD5	J21	26	POD_B_EVEN5	C25
27	POD_B_ODD4	K26	28	POD_B_EVEN4	D25
29	POD_B_ODD3	K25	30	POD_B_EVEN3	E25
31	POD_B_ODD2	K24	32	POD_B_EVEN2	F26
33	POD_B_ODD1	K23	34	POD_B_EVEN1	F25
35	POD_B_ODD0	K22	36	POD_B_EVEN0	G26
37	3.3 V	N/A	38	5.0 V	N/A
39	GND	N/A	40	GND	N/A

Axcelerator Platform Development Kit Contents and Uninstall

Development Kit Contents

The contents of the Axcelerator Platform Development Kit are shown in [Figure A-1](#).

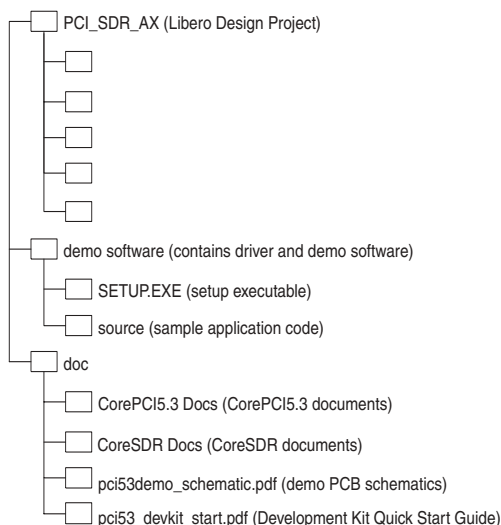


Figure A-1. Axcelerator Platform Development Kit Contents

Note: The sample source code for the software demo is provided for reference only. Actel does not provide user support for this code.

Removing the PCI Demo Board

To uninstall the demo board:

1. Shut down your PC.
2. Remove the PCI Development Board using static-safe procedures.
3. Boot your PC. Log in as Administrator if required.
4. Remove the software. Go to **Control Panel > Add or Remove Programs**, select **Actel PCI**, then click **Remove**.
5. Reboot if required.

CorePCI and CoreSDR Parameters

CorePCI was programmed with the parameters shown in [Table B-1](#). The CoreSDR parameters are shown in [Table B-2 on page 34](#).

Table B-1. CorePCI Parameters

Parameter	Programmed Value	Range		Description
		From	To	
PCI_WIDTH	32	32	64	Sets whether to use a 32- or 64-bit PCI implementation (must be 32 or 64)
PCI_FREQ	66	33	66	Sets whether core supports 66 MHz operation (must be 33 or 66)
TARGET	1	0	1	When 1, the PCI Target function is implemented.
MASTER	1	0	1	When 1, the PCI Master function and DMA controller are implemented.
BACKEND	0	0	1	When 1, the backend interface to the DMA control registers is enabled. When 0, the DMA registers can only be accessed from the PCI bus. If BACKEND = 1 and DMA_REG_LOC > 0, the DMA control registers can be accessed from both the PCI and backend interfaces.
SLOW_READ	0	0	1	When 1, the core is only capable of transferring data every other clock cycle but requires less FPGA resources. This must be 0 when the FIFO recovery function is enabled.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
DMA_REG_LOC	2	0	3	<p>Configures how the DMA control registers are accessed from the PCI bus.</p> <p>0: None—Access is not allowed; the registers must be accessed from the backend.</p> <p>1: Config—DMA registers are mapped to locations 50–5F hex of the configuration space.</p> <p>2: MEM—DMA registers are mapped to configuration space and memory locations 50–5F hex of the BAR set by DMA_REG_BAR.</p> <p>3: IO—DMA registers are mapped to configuration space and I/O locations 50–5F hex of the BAR set by DMA_REG_BAR.</p>
DMA_REG_BAR	2	0	5	<p>Sets which BAR is used to access the DMA registers. If DMA_REG_LOC is 2 or 3, the BAR parameters must be set up to configure a 256–byte BAR using either memory or I/O mapped with prefetch disabled.</p>
DMA_COUNT_WIDTH	25	0	32	<p>Sets the width of the internal DMA counter. If set to 12, the DMA engine can transfer up to 2,048 bytes of data.</p> <p>Max. Transfer Size = $2^{\text{DMA_COUNT_WIDTH}}$</p>

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
VENDOR_ID	4522	0	65535	Sets the user vendor ID value in the PCI configuration space. The Actel vendor ID is 4522 (11AA hex) and may be used with permission from Actel, which will allocate a device ID and sub-vendor ID on demand.
DEVICE_ID	24582	0	65535	Sets the user device ID value in the PCI configuration space
REVISION_ID	96	0	255	Sets the device ID value in the PCI configuration space
BASE_CLASS	5	0	255	Sets the base class value in the PCI configuration space
SUB_CLASS	0	0	255	Sets the sub-class value in the PCI configuration space
PROGRAM_IF	0	0	255	Sets the program interface value in the PCI configuration space
SUBVENDOR_ID	4522	0	65535	Sets the sub-vendor ID value in the PCI configuration space
SUBSYSTEM_ID	24582	0	65535	Sets the sub-system ID value in the PCI configuration space
CIS_UPPER	0	0	65535	Sets the value of the upper 16 bits of the CardBus CIS Pointer
CIS_LOWER	0	0	65535	Sets the value of the lower 16 bits of the CardBus CIS Pointer
MINMAXLAT	32	0	65535	Sets the minimum grant and maximum latency values at location 3E hex in the configuration space

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
BAR0_ENABLE	1	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
BAR0_ADDR_WIDTH	25	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR0_ADDR_WIDTH}$
BAR0_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space
BAR0_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.
BAR1_ENABLE	1	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
BAR1_ADDR_WIDTH	13	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR1_ADDR_WIDTH}$
BAR1_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space
BAR1_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
BAR2_ENABLE	1	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
BAR2_ADDR_WIDTH	8	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR2_ADDR_WIDTH}$
BAR2_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space
BAR2_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.
BAR3_ENABLE	0	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
BAR3_ADDR_WIDTH	4	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR3_ADDR_WIDTH}$
BAR3_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space
BAR3_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
BAR4_ENABLE	0	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery.
BAR4_ADDR_WIDTH	4	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR4_ADDR_WIDTH}$
BAR4_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space
BAR4_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.
BAR5_ENABLE	0	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
BAR5_ADDR_WIDTH	4	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR5_ADDR_WIDTH}$
BAR5_IS_IO	0	0	1	0: BAR is configured as memory space 1: BAR is configured as I/O space.
BAR5_PREFETCH	0	0	1	If BAR is Memory space, this bit controls the PREFETCH bit in the base address register. This should be set to zero when the FIFO recovery logic is enabled.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
EXPR_ENABLE	0	0	2	0: Bar is disabled 1: Bar is enabled 2: Bar is enabled with FIFO recovery
EXPR_ADDR_WIDTH	8	4	31	Specifies the width of the base address register. If the BAR is disabled, this should be set to 4. $BAR_SIZE = 2^{BAR0_ADDR_WIDTH}$
ENABLE_HOT_SWAP	0	0	1	Enables the hot swap register and functionality
ENABLE_DIRECTDMA	0	0	1	When 1, direct DMA mode is enabled, allowing the PCI data value to be read from and written to an internal register rather than the backend interface.
DISABLE_WDOG	0	0	1	When 1, data transfer watchdog inside the core is disabled. The core normally includes a transfer watchdog that will terminate a PCI cycle if the backend logic fails to provide or accept data within the time limits defined by the PCI specification. Some embedded systems may wish to disable this function if longer access times are permitted.
DISABLE_BAROV	0	0	1	When 1, the core will not disconnect when a memory or I/O transfer overflows the BAR, as required by the PCI specification. Instead, the core will wrap the address and jump to the beginning of the BAR space. Setting the parameter to 1, will reduce the number of logic elements that the core requires.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
MADDR_WIDTH	25	4	32	Specifies the width of the backend address bus. This should match the largest set BAR address width. For example, if 64 kbytes of address space is configured, MADDR_WIDTH should be set to 16.
USE_GLOBAL_RESET	1	0	1	When 1, a global buffer is used to drive the internal reset work. When 0, a global buffer is not used, allowing the global to be used for other clock networks, etc., within the design.
CMD_INITVAL	0	0	65535	When 1, a global buffer is used to drive the internal reset work. When 0, a global buffer is not used, allowing the global to be used for other clock networks, etc., within the design.
BAR0_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 0. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance the generic should be set to zero.
BAR1_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 1. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance, the generic should be set to zero.
BAR2_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 3. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance, the generic should be set to zero.

Table B-1. CorePCI Parameters (Continued)

Parameter	Programmed Value	Range		Description
		From	To	
BAR3_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 4. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance, the generic should be set to zero.
BAR4_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 4. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance, the generic should be set to zero.
BAR5_INITVAL	0	0	268435455	Specifies the reset value of the top 28 bits of BAR 5. This allows a BAR address space to be active immediately after reset. To maintain PCI compliance, the generic should be set to zero.

Table B-2. Top-Level CoreSDR Programmed Parameters/Generics

Parameter/Generic	Programmed Value	Description
sdram_rasize	31	Local address bus size
sdram_chips	2	Number of chip selects
sdram_banks	4	Number of SDRAM banks
sdram_colbits	9	Number of SDRAM column bits
sdram_bankbits	2	Number of SDRAM bank bits
sdram_rowbits	14	Number of SDRAM row bits
sdram_chipbits	3	Number of encoded chip select bits
sdram_bank stat modules	1	Number of bank status modules used (in multiples of 4)

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**

From Southeast and Southwest U.S.A., call **650.318.4480**

From South Central U.S.A., call **650.318.4434**

From Northwest U.S.A., call **650.318.4434**

From Canada, call **650.318.4480**

From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**

From Japan, call **650.318.4743**

From the rest of the world, call **650.318.4743**

Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the [Actel Customer Support website \(www.actel.com/custsup/search.html\)](http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's [home page](http://www.actel.com), at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460

800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. [Sales office listings](#) can be found at www.actel.com/contact/offices/index.html.

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For more information about Actel's products, visit our website at <http://www.actel.com>

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