



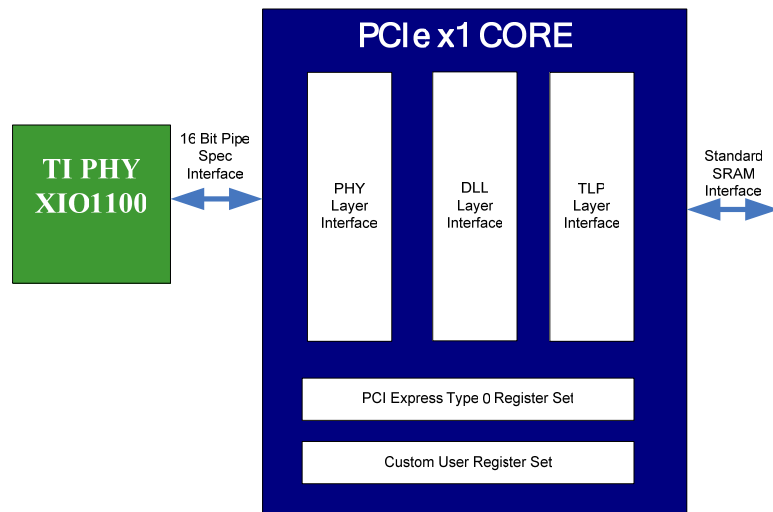
# PCI Express Core

## Product Features

### General Features

- Designed specifically for the Actel ProAsic and TI XIO1100
- Meets timing and uses ~50% of the Actel A3P1000 device
- Pci Express Base specification endpoint compliant
- 16 bit 125 MHz Pipe spec interface
- Master and Slave PCIe capability
- Standard SRAM interface to the transaction layer
- PHY, DLL, TL Layers
- PCI Type 0 configuration register set
- Custom configuration register set
- Link and device power management
- PCIe verilog testbench available
- PCIe Demo Board available

## PCI Express x1 TI PHY SRAM IF



### PCIe Features

#### Physical Layer

- 16 bit Pipe Specification interface including detect and power management
- 16 bit scrambler algorithm for scrambling the TX data and de-scrambling the RX data.
- LTSSM state machine
- Link training TS1, TS2 link and lane negotiation
- L0s, L1 power management control

#### Data Link Layer

- Credit Control and Initialization
- LCRC generator and checker
- Ack/Nack generation and processing
- Replay Buffer
- Sequence number generator and checker

#### Transaction Layer

- Up to 2K max packet size support
- Data and header queue management
- Transaction ordering rule compliant
- Configurable BAR address decoding and packet rejection

#### Transaction Layer(Cont)

- Error checking including malformed packet
- Tlp support for Cfg0Wr/Rd MWr/Rd and IOWr/Rd transaction types

#### Internal Registers

- Type 0 configuration register set including MSI, PCIe, and PowerManagement capability registers
- Custom configuration registers including doorbell, scratch pad and internal buffer space

#### Standard SRAM Interface Features

- Separate 32 bit wide data bus
- Separate 16 bit wide address bus
- Byte enable support and PCIe byte enable rule checking
- Provides a 62.5 MHz SRAM clock
- Continuous data bursting to length of packet