Product Brief
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1 Introduction

The IEEE 802.3 Ethernet Standard defines a medium independent interface for all speeds ranging from 10 MBit/s to 10GBit/s.

Besides the data interface, a two-wire Management Interface (MDIO) is defined to connect MAC devices with PHY devices providing a standardized access method to internal registers of PHY devices.

The MDIO is a shared bus structure shared offering up to 32 devices to be connected to the interface. All data is transferred clock synchronously to the Management Data Clock (MDC) which is provided by the MAC and sourced to all receiving devices. The data line is a shared tri-stateable bus, which is driven by the MAC for write transactions or by the PHY devices during a read transaction. The MDIO interface clock (MDC) speed is defined for up to 2.5 MHz.

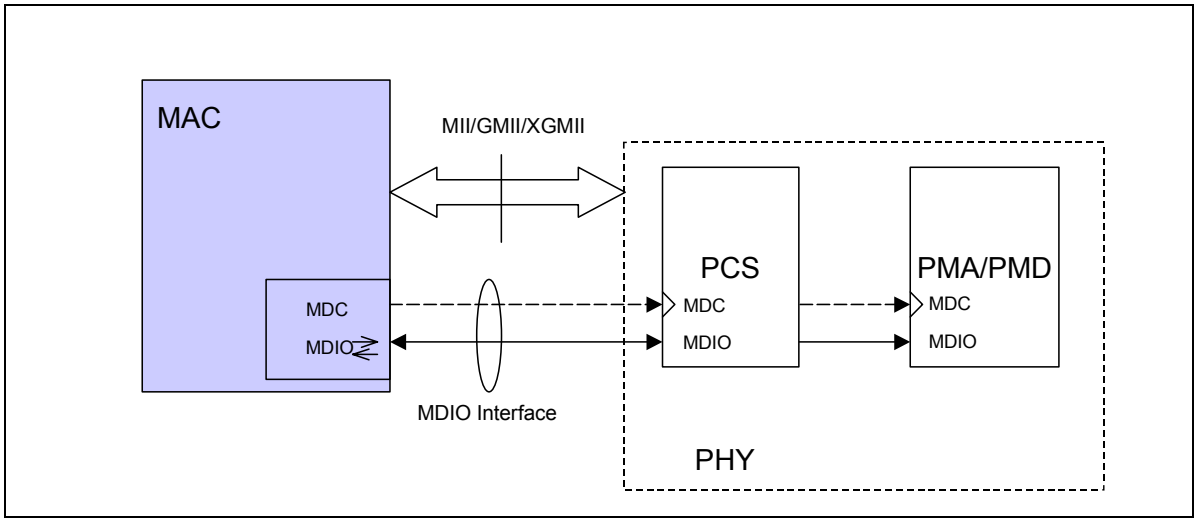

Figure 1: MDIO Application

The Master core is usually embedded in the Ethernet MAC and handles parallel to serial conversion and is responsible for all read and write transactions from and to the Slave devices. The Master provides three registers to implement the procedures for accessing connected Slave (PHY) registers. A host processor responsible for system configuration and monitoring typically uses the MDIO master to perform individual accesses to the various devices.

2 MDIO Master Core Features

- Implements the IEEE 802.3 Clause 22 standard MDIO interface used in Ethernet systems up to 1Gbit/s
- MAC Layer (Master) core allowing access to registers within multiple connected Slaves
- Simple register based user application interface for the Master cores
- Automatic transaction MDIO frame generation with serial port tristate control and busy indication to user application during ongoing transaction

3 Implementation Summary

Table 1: MDIO Master core Implementation

Axcelerator Device	Speed Grade	Complexity (With 512-Byte FIFOs)				Performance	Requirement
		C-Cells	R-Cells	Total Utilization	RAM		
AX500	std	95 (2%)	73 (3%)	3%	-	>107MHz	2.5MHz

Table 2: Implementation Summary - ProASICplus

ProASICplus Device	Speed Grade	Complexity (With 512-Byte FIFOs)		Performance	Requirement
		Cells (Total Utilization)	RAM		
APA075	std	256 (8%)	-	>79MHz	2.5MHz

4 MDIO Design Kit Overview

Table 3: Design Database Overview

Design and Simulation	
Language	VHDL / Verilog or netlist for Actel FPGA implementation.
Simulation	Testbench with embedded MDIO frame checker and user application interface control, providing an easy to use and robust debugging environment.
Verification	Comprehensive test environment with MDIO frame validation and user application transaction stimulation and verification.
Design Tools	
Simulation	Modelsim Version 5.4d or higher
Synthesis	Exemplar Leonardo Spectrum 2002c or higher Synplicity Synplify 7.1 or higher
Implementation	Actel Libero IDE (Integrated Design Environment) V2.2 or higher, or Actel Designer R1-2002 or higher.

5 Ordering Code

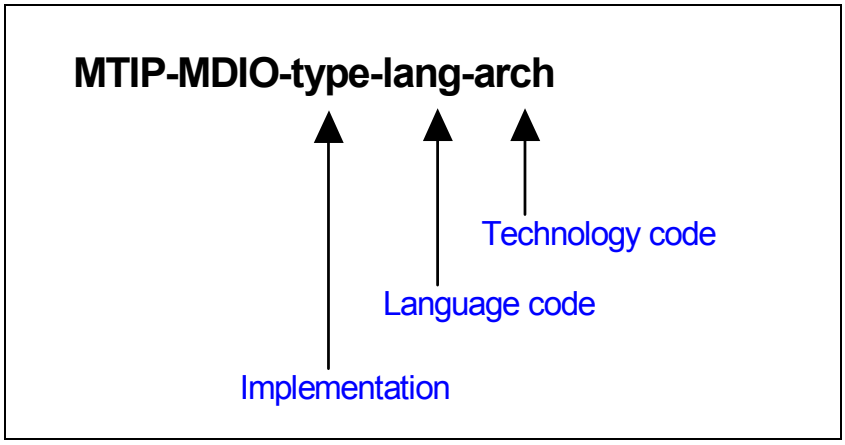

Table 4: Implementation Type

Implementation Code	Description
M	MDIO Master

Table 5: Language Code

Technology Code	Target Technology
BIN	Binary netlist for Actel Axcelerator or ProASIC$_{plus}$ FPGAs.
VHDL	Synthesizable generic VHDL source code for Actel Axcelerator or ProASIC$_{plus}$ FPGAs or ASIC implementations
VLOG	Synthesizable generic Verilog source code for Actel Axcelerator or ProASIC$_{plus}$ FPGAs or ASIC implementations

Table 6: Technology Code

Technology Code	Target Technology
GEN	Source code option for Actel Axcelerator or ProASIC$_{plus}$ FPGAs or ASIC implementations.
ACTL	Netlist for Actel Axcelerator or ProASIC$_{plus}$ FPGAs.

6 References

1. Clause 22 MDIO, IEEE 802.3 2000 Edition

7 Contact

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