

AvnetCore: Datasheet

Version 1.0, July 2006

CAN Controller with TX/RX FIFO

Intended Use:

- Automotive Industry
- Engine Control Unit
- Sensors

Features:

- CAN 2.0B, 1Mbit/s
- Very small (2066 tiles in ProASIC^{PLUS}[®] and 1847 tiles in ProASIC3)
- Fully Synchronous Design
- Independent clocks for APB and XCAN
- AMBA (APB) compliant interface
- RX/TX FIFO controller
- Configurable FIFO size

Targeted Devices:

- Axcelerator[®] Family
- ProASIC^{PLUS}[®] Family

Core Deliverables:

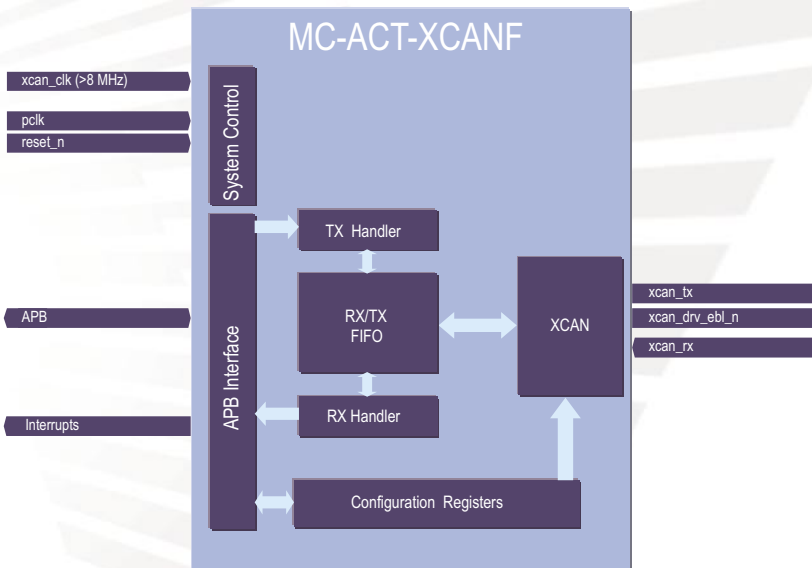
- Netlist Version
 - > Netlist compatible with the Actel Designer place and route tool
- RTL Version
 - > VHDL Source Code
 - > Test Bench
- All
 - > User Guide

Synthesis and Simulation Support:

- Synthesis: Synplicity[®]
- Simulation: ModelSim[®]
- Other tools supported upon request

Verification:

- Test Bench



Logic Symbol

Controller Area Network (CAN) is a serial network that was originally developed for the automotive industry, and has become a popular in industrial automation as well as other applications. As its name implies, CAN is a network established among multiple controllers. It is a two-wire, half duplex, high-speed network that is well suited for applications using short messages. Its robustness, reliability and wide spread use are among its benefits. A CAN bus can theoretically link over 2000 devices on a single network, but real world hardware is limited to something on the order of 100 nodes. It offers communication at up to 1 Mbits/sec, and thus allows real-time control for many applications. In addition, CAN error handling make it more reliable in high noise environments. The MC-ACT-XCANF is an APB compliant full CAN controller with a very small FPGA 'footprint'. It provides a transmission and a reception FIFO of configurable size, including FIFO controllers. The independent clocks give maximum flexibility. The configuration registers can be fixed for lowest resource requirements or implemented as ordinary read/write registers. Both FIFO size and configuration register behavior can be defined via generics. The RX and TX interrupts allow an efficient message handling.

Functional Description

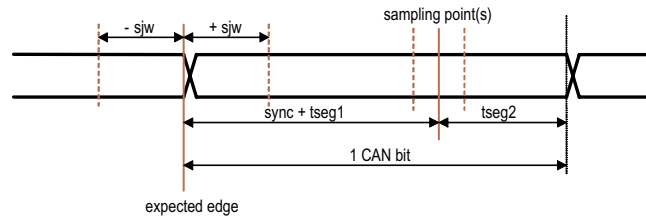
The XCAN core contains the complete data link layer, including the framer, transmit and receive control, error handling, error reporting and synchronization. The core is designed to provide a bus bit rate up to 1Mbit/s with a minimum core clock frequency of 8 MHz.

CAN CONFIGURATION

Bit rate, sub-bit segments (timing segment 1 & 2) and the synchronization jump width (sjw) for resynchronization can be configured to meet the required timing to the connected CAN bus.

The edge for resynchronization on the incoming message is defined in the edge-mode. Either the R-D edge or both (R-D and D-R) are used for resynchronization. The XCAN provides two different sampling modes: Direct Sampling or three point sampling with majority decision.

The following diagram shows the bit timing:

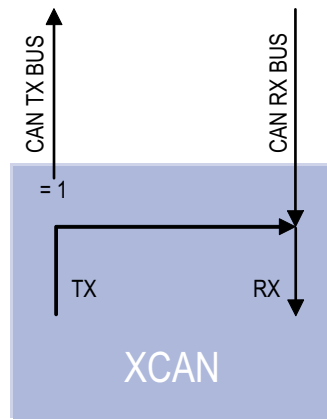


START/STOP CONTROLLING

The XCAN can be set in stop or start mode by user command.

SILENT MODE

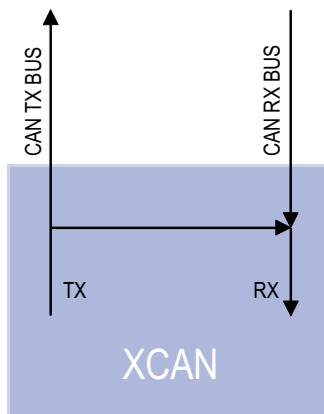
In silent mode the XCAN receives valid data and remote frames but sends only recessive bits on the CAN bus. In this mode the bus traffic can be analyzed without affecting it by sending dominant bits. The tx bus of the core is internally routed to the rx bus to receive acknowledges generated by this core.



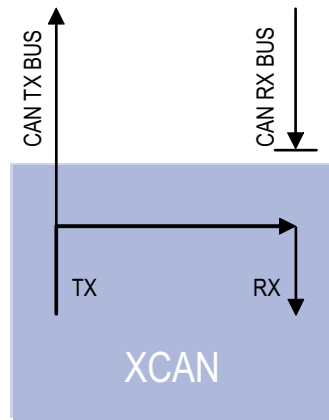
LOOP BACK MODE

In loop back mode the XCAN receives also messages which are sent by the core itself. Two different loop back mode can be configured.

Mode a: The core receives also messages sent by itself.



Mode b: The CAN receives only messages sent by itself and ignores messages and acknowledges from CAN rx bus.



SILENT MODE COMBINED WITH LOOP BACK MODE

Loop back and silent mode can be used together. In this configuration the XCAN can be tested without affecting a running CAN system.

Functional Description

CLOCK CONFIGURATION

The MC-ACT-XCANF has two independent clock inputs, one for the APB interface and one for the XCAN core. This makes the core very flexible, connecting it to a fast APB bus while the XCAN runs on a clock > 8MHz. Of course these two clocks can also be fed from the same source.

APB INTERFACE

The core comes with an AMBA (APB) compliant interface. The APB protocol is very simple and the interface can be easily used as a generic interface. Message handling, configuration of the core and read out of status information is done via this interface. For more information about the registers and address offsets please refer the user guide.

TX HANDLER

For transmission the MC-ACT-XCANF provides TX FIFO of configurable size. From the software point of view the TX FIFO looks like a small memory for 1 message only. The software can write the message to the FIFO in any order; ID, data and so on. To commit the message to the FIFO only a write access is required. From now on the FIFO plus the XCAN take care of sending the message onto the CAN network

As soon as a message has been transmitted completely a TX interrupt flag is set to mark this event. In addition one can also read back the TX FIFO fill level at any time to schedule transmission. The TX handler also takes care of overflow protection. A write access to the full TX FIFO is ignored, keeping the messages already in the FIFO valid. An overflow is marked with a TX overflow flag that keeps active until it is cleared explicitly.

RX HANDLER

The RX handler works very much the same as the TX handler. The software sees the RX message as if it was reading it from a small memory. Once the RX message has been read it needs to be acknowledged. After that it is removed from the FIFO. In case the software cannot keep up reading out the RX messages an overflow flag marks the event of an overflow. Again, if the RX FIFO is full following messages will be ignored leaving the messages already in the FIFO valid.

INTERRUPTS

The MC-ACT-XCANF provides 3 interrupts for efficient message and CAN error handling. One flag marks the reception of a new RX message, one marks that a message has been completely sent and the third flag signals that either the RX or the TX error counter or both have become bigger than 96.

Device Requirements

Family	Device	Utilization				Performance
		COMB	SEQ	Total	RAM Blocks	pclk/xcan_clk
Axcelerator	A3P250-2	15%	8%	1847 (30%)	8 (64 tx / 64 rx)	77/28 MHz
ProASIC ^{PLUS}	APA075-STD	n/a	n/a	2066 (67%)	8 (64 tx / 64 rx)	54/16 MHz
ProASIC3	APA450-BG456	765 (57%)	210 (31%)	975 (49%)	2 (32 tx / 32 rx)	102/22 MHz

Table 1: Device Utilization and Performance

Verification and Compliance

Functional and timing simulation has been performed on the MC-ACT-XCANF using VHDL Test Benches. Simulation vectors used for verification are provided with the core. This core has also been used successfully in customer designs.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
RESET_N	Input	Asynchronous system reset, active low
XCAN_CLK	Input	Clock source for the XCAN, > 8 MHz
PCLK	Input	APB clock
PADDR[31:0]	Input	APB Address input, bits [5:2] used only
PSEL	Input	APB Select signal
PENABLE	Input	APB Enable signal
PWRITE	Input	APB Write signal
PWDATA[31:0]	Input	APB Write data
PRDATA[31:0]	Output	APB Read data
PDATA_BYTE_EBL[3:0]	Input	Data byte enable
XCAN_INT_TX	Output	Transmit interrupt
XCAN_INT_RX	Output	Receive interrupt
XCAN_INT_ERR	Output	Error counter >= 96 interrupt
XCAN_RX_BUS	Input	Receiver pin of CAN bus
XCAN_TX_BUS	Output	Transmitter pin of CAN bus
XCAN_BUS_EBL_N	Output	Can bus driver enable; '0': active, '1': passive

Table 2: Core I/O Signals

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero v2.2 Integrated Design Environment (IDE) and preferably with Synplify and ModelSim.

Ordering Information

The CORE is provided under license from Memec Design for use in Actel programmable logic devices. Please contact Memec Design for pricing and more information.

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Ordering Information:

Part Number

MC-ACT-XCANF-NET
MC-ACT-XCANF-VHD

Hardware

Actel Core Netlist
Actel Core VHDL

Resale

Contact for pricing
Contact for pricing



www.em.avnet.com/actel