

Overview

Universal Test and Operations Interface for ATM (UTOPIA) defines the interface between the physical layer (PHY) and upper layer modules such as the asynchronous transfer mode (ATM) layer and various management entities. The definition allows a common PHY interface in ATM subsystems across a wide range of speeds and media types. These interfaces target cell-based communications applications, including ATM systems, high-speed port adapters for ATM switches, routers, remote access concentrators, and up-links. Please refer to ATM Forum documents for detailed descriptions of the interface.

UTOPIA 2 is intended to service data rates up to 622 Mbps (OC-12). It extends the UTOPIA 1 specification in three ways: 1) it allows single or multiple logical PHY ports on a single PHY layer device to be connected to one or more link layer devices, 2) it adds the 16-bit data path and 54 octet cells, and 3) it increases clock rate to support higher data throughput from OC-3 (155 Mbps). Because of the UTOPIA specification's built-in backward compatibility, the UTOPIA 2 (UL2) core described herein was also designed to address UTOPIA 1 applications.

General Description

Both master and slave UL2 cores are available from Memec Design. With modular architecture, the core allows users to replace the supplied FIFO with custom FIFO blocks (change

depth, use off-chip RAM, etc.). It may allow cheaper FPGAs to be employed. Also, the ingress and egress modules may be separated into different chips.

All Memec Design telecom core offerings are constructed with the same no-nonsense user interface and architecture.

The supplied FIFO block allows breaking clock domains within the core. The FIFO block can be run with different clocks on the user interface side and the UL2 interface side. For example, the user FIFO interface can run faster or slower than the interface clock.

To gain complete control over the core configuration, the user can adjust the parameters in the top-level source file, which also allows the core to be easily modified and reused. These parameters include data bus width, SPHY/MPHY, number of PHY ports and cell size.

In SPHY mode, the addressing state machine (for the master/ATM layer core) or address decoder (for the slave/PHY layer core) is discarded, which results in optimal usage of device resources.

The cores come with a testbench to aid the customer with integration. The PHY core comes with a simulation version of the LINK core, and the LINK core comes with a simulation version of the PHY core. The testbench allows the customer to simulate many types of traffic patterns, enabling the designer to evaluate flow control and port polling fairness in their application scenario.

Features

- Compliant with ATM Forum af-phy-0039.0000
- Simple system side FIFO interface
- Asynchronous or synchronous FIFOs using block RAM
- Supports up to 31 PHYs
- Supports both 8- and 16-bit interfaces
- 25, 33, and 50 MHz clock rates
- Supports 52, 53, and 54 octet cells
- Automatic PHY polling and selection

Applications

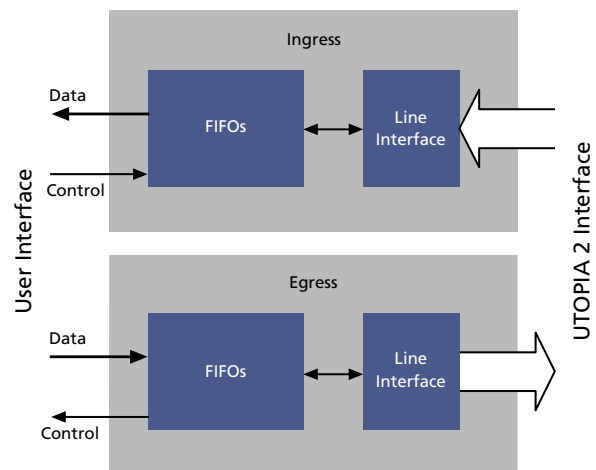
- ATM cell processors
- AAL SARs
- Framers
- ATM switch fabrics

Target Technology

Embedding the UTOPIA 1 and 2 cores in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products.

The UTOPIA 1 and 2 cores support many Actel devices, including:

- Axcelerator



About Memecore™ Products

Memecore™ intellectual property (IP) cores comprise a vital element of the Memec Design portfolio. Expert designers create each core with the target silicon in mind, which ensures an optimal implementation. This practice translates into significant costs savings over comparable solutions that require more silicon and faster speed grades. Visit www.memecdesign.com/actel to review the current list of released cores and other available IP.



UTOPIA 1 and 2

Optimized for Actel

Questionnaire

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

Contact Information:

Name: _____ E-mail: _____

Company: _____ Phone: _____

Address: _____

City: _____ State: _____ Zip: _____ Job Title: _____

Pricing:

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?

Yes No Unknown

Evaluation / Implementation:

What is your preferred design language?

VHDL Verilog Other: _____

What is your simulation environment?

ModelSim NC-Verilog NC-VHDL NC-Sim Verilog-XL Scirocco VCS VSS Other: _____

What is your synthesis environment?

FPGA Express Leonardo Spectrum Synplify FPGA Compiler II BuildGates Design Compiler Other: _____

What is your Actel implementation environment?

Libero Silver Libero Gold Libero Platinum Designer Gold Designer Platinum Other: _____

What is your target Actel family?

Axcelerator Other: _____

Customization / Integration:

Do you have a design specification? Yes No

Describe your application: (attach a block diagram if possible) _____

Other Information:

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To contact the local Memec distributor who sells and supports Actel, go to www.memecdesign.com/actel