

Overview

The two-wire serial interface (TWSI) bus is a simple two-wire bus that allows microcontrollers to connect to specialized ICs like EEPROMS and system monitoring hardware. Simplicity of the TWSI bus system is primarily due to the bi-directional two-wire design using a serial data line (SDA) and serial clock line (SCL). Each device on the TWSI bus is recognized by a unique 7-bit address and can operate as a transmitter or as a receiver. In addition to transmitter and receiver, the TWSI bus uses the concept of master and slave. The TWSI bus allows for a multimaster system, which means more than one device can initiate data transfers at the same time.

General Description

The TWSI solution can be configured to operate in three modes: master only (MO), slave only (SO), or both master and slave (MS). The TWSI core is specifically designed for Actel FPGAs and emulates the functionality of the industry-standard two-wire serial interface supporting multiple masters. The core does not support 10-bit slave addressing or START byte data transfers. The core facilitates upgrading current systems by allowing the designer to incorporate the TWSI function as well as other logic into a single, state-of-the-art FPGA. The core is designed such that it can be instantiated into an Actel design, connected to the design's logic, and compiled to make a device that will "plug in" to a TWSI application.

Features

- I²C-compatible two-wire serial interface core
- Multimaster operation with arbitration and clock synchronization
- Slave transmit and receive operation
- Support for reads, writes, burst reads, burst writes, and repeated start
- User-defined timing and clock frequency
- Fast mode and standard mode operation

Applications

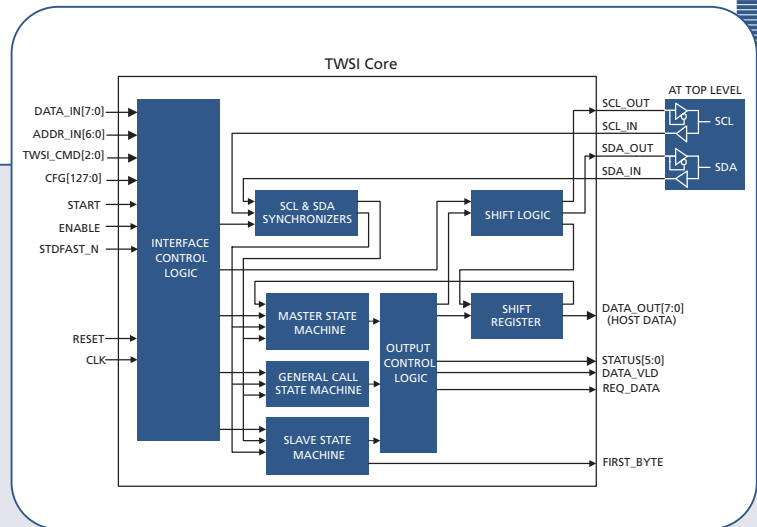
- Embedded microprocessor boards
- Any circuit needing I²C peripherals (I²C is a trademark of Philips, Inc.)

Target Technology

Embedding the TWSI cores in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products.

The TWSI core supports many Actel devices, including:

- Axcelerator
- ProASIC^{PLUS}



About Memecore™ Products

Memecore™ intellectual property (IP) cores comprise a vital element of the Memec Design portfolio. Expert designers create each core with the target silicon in mind, which ensures an optimal implementation. This practice translates into significant costs savings over comparable solutions that require more silicon and faster speed grades. Visit www.memecdesign.com/actel to review the current list of released cores and other available IP.





TWSI Controller

Optimized for **Actel**

Questionnaire

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

Contact Information:

Name: _____ E-mail: _____

Company: _____ Phone: _____

Address: _____

City: _____ State: _____ Zip: _____ Job Title: _____

Pricing:

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?

Yes No Unknown

Evaluation / Implementation:

What is your preferred design language?

VHDL Verilog Other: _____

What is your simulation environment?

ModelSim NC-Verilog NC-VHDL NC-Sim Verilog-XL Scirocco VCS VSS Other: _____

What is your synthesis environment?

FPGA Express Leonardo Spectrum Synplify FPGA Compiler II BuildGates Design Compiler Other: _____

What is your Actel implementation environment?

Libero Silver Libero Gold Libero Platinum Designer Gold Designer Platinum Other: _____

What is your target Actel family?

Accelerator ProASIC^{PLUS} Other: _____

Customization / Integration:

Do you have a design specification? Yes No

Describe your application: (attach a block diagram if possible) _____

Line Interface (front-end) Information

What is your data rate? 100 Kbps 400 Kbps

Bus Interface (back-end) Information

What is your bus interface? _____

Other Information:

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