Memec Design

POS-PHY Level 3 (SPI3)

Limited Release

Optimized for Actel

Overview

POS-PHY Level 3 (PL3) is an industry standard interface endorsed by the ATM Forum to transfer data between framers and PHY devices. Level 3 is intended to service data rates up to 2.488 Gbps (OC-48). In addition to transporting ATM cells, the PL3 interface also facilitates Packet over SONET (POS) implementation in applications where the packet length may be variable.

The PL3 interface allows one PHY layer device to connect to one link layer device, and, when joined in this manner, supports single or multiple logical PHY ports. The PL3 specification defines both the physical implementation of the bus and the signaling protocol used to communicate data.

General Description

Both LINK and PHY PL3 cores are available from Memec Design. With modular architecture, the cores allow users to replace the supplied FIFO with custom FIFO blocks (change depth, use off-chip RAM, etc.). This may allow cheaper FPGAs to be employed. Also, the ingress and egress modules may be separated into different chips.

All Memec Design telecom core offerings are constructed with the same no-nonsense user interface and architecture.

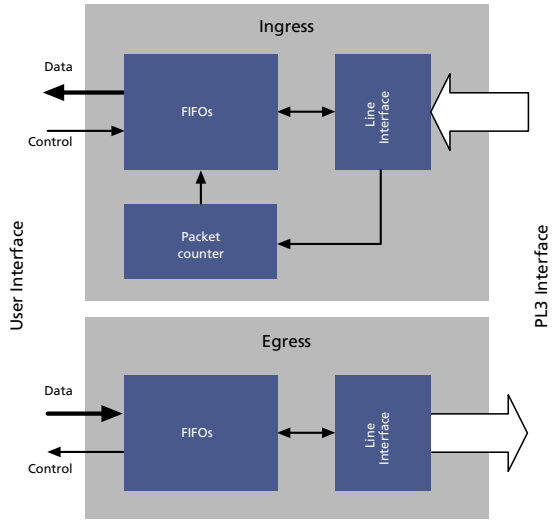
The supplied FIFO block permits breaking clock domains within the core. The FIFO block can be run with different clocks on the user interface side and the PL3 interface side. For example, the user FIFO interface can run faster or slower than the PL3 interface clock.

To gain complete control over the core configuration, the user can adjust the parameters in the top-level source file, which also allows the core to be easily modified and reused. These top-level source file parameters include data bus width, SPHY/MPHY, number of PHY ports, direct/polled status, high watermark, and burst size. In SPHY mode, the addressing state machine (for the LINK core) or address decoder (for the PHY core) is discarded, which results in optimal usage of device resources.

The adjustable high watermark regulates the "almost full" condition, whereas the burst size parameter specifies maximum data burst across the PL3 interface per port.

Included with the cores, a testbench aids the customer with integration. The PHY core comes with a simulation version of the LINK core, and the LINK core comes with a simulation version of the PHY core. The testbench allows the customer to simulate many types of traffic patterns, allowing the designer to evaluate flow control and port polling fairness in their application scenario.

Also included, a Windows® based GUI configurator aids in core customization.



MemecCore™ Intellectual Property

Features

- Compliant with ATM Forum af-phy-0143.000
- Supports both 8-bit and 32-bit interfaces
- Also supports nonstandard 16-bit interface
- Simple system-side FIFO interface
- Asynchronous or synchronous FIFOs
- Supports up to 256 PHYs
- Programmable high and low watermarks on FIFO
- Supports both direct status and polled status flow control methods
- Automatic PHY polling and selection

Applications

- Packet processors
- UNI/MAC
- Framers
- PHYs/framer interfaces

Target Technology

Embedding the POS-PHY Level 3 LINK and PHY cores in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products.

The POS-PHY Level 3 LINK and PHY cores support many Actel devices, including:

- Axcelerator

About MemecCore™ Products

MemecCore™ intellectual property (IP) cores comprise a vital element of the Memec Design portfolio. Expert designers create each core with the target silicon in mind, which ensures an optimal implementation. This practice translates into significant costs savings over comparable solutions that require more silicon and faster speed grades. Visit www.memecdesign.com/actel to review the current list of released cores and other available IP.

Actel CompanionCore

Memec Design

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Questionnaire

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

Contact Information:

Name: _____ E-mail: _____

Company: _____ Phone: _____

Address: _____

City: _____ State: _____ Zip: _____ Job Title: _____

Pricing:

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?

☐ Yes ☐ No ☐ Unknown

Evaluation / Implementation:

What is your preferred design language?

☐ VHDL ☐ Verilog ☐ Other: _____

What is your simulation environment?

☐ ModelSim ☐ NC-Verilog ☐ NC-VHDL ☐ NC-Sim ☐ Verilog-XL ☐ Scirocco ☐ VCS ☐ VSS ☐ Other: _____

What is your synthesis environment?

☐ FPGA Express ☐ Leonardo Spectrum ☐ Synplify ☐ FPGA Compiler II ☐ BuildGates ☐ Design Compiler ☐ Other: _____

What is your Actel implementation environment?

☐ Libero Silver ☐ Libero Gold ☐ Libero Platinum ☐ Designer Gold ☐ Designer Platinum ☐ Other: _____

What is your target Actel family?

☐ Axcelerator ☐ Other: _____

Customization / Integration:

Do you have a design specification? ☐ Yes ☐ No

Describe your application: (attach a block diagram if possible) _____

Other Information:

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To contact the local Memec distributor who sells and supports Actel, go to www.memecdesign.com/actel