Overview

The acceptance of the Internet has led to a dramatic rise in data traffic. To successfully transmit data over any network, a protocol is required to manage the flow or pace at which the data is transmitted. This protocol is defined in Layer 2 of the industry standard communication reference model called OSI (Open Systems Interconnection). High-Level Data Link Control (HDLC) is the most commonly used Layer 2 protocol and is a bit-oriented synchronous data link layer protocol developed by the International Standards Organization (ISO).

The HDLC core is designed specifically for FPGAs and provides the HDLC frame structure. The design is intended to be integrated with some type of buffer packet storage, either FIFO or DMA memory, for both transmitting and receiving. The transmitter and receiver are two totally independent blocks with separate clocks, allowing separate transmit and receive data rates.

General Description

The HDLC core performs the most common functions of an HDLC controller. Data bytes are clocked into the device, based on a divided version of the transmit clock. This data is then serialized and framed according to the rules of HDLC and sent out the serial transmit data pin. Receive frames are clocked into the receive data pin synchronous to the receive clock. The framing overhead is then stripped off and the data bytes are converted from serial to parallel and passed on through the parallel receive bus.

Features

- Conforms to International Standard ISO/IEC 3309 specification
- 16-bit/32-bit FCS generation and checking
- Flag and zero insertion and detection
- Full-duplex operation
- DC to 53 Mbps (STS-1) data rate
- Fully synchronous operation
- Selectable idle of flags or all logic ones

Applications

- Frame relay switches
- ISDN
- X.25 and V.35 protocols
- T1/E1, T3/E3 applications
- Internet/edge routers, bridges, and switches
- Cellular basestation switch controller
- xDSL
- Multiplexers/concentrators

Target Technology

Embedding the single-channel HDLC core in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products. The HDLC core supports many Actel devices, including:

- Accelerator
- ProASICplus

About MemecCore™ Products

MemecCore™ intellectual property (IP) cores comprise a vital element of the Memec Design portfolio. Expert designers create each core with the target silicon in mind, which ensures an optimal implementation. This practice translates into significant costs savings over comparable solutions that require more silicon and faster speed grades. Visit www.memecdesign.com/actel to review the current list of released cores and other available IP.
**Questionnaire**

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

**Contact Information:**

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<tr>
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**Pricing:**

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?
- [ ] Yes
- [ ] No
- [ ] Unknown

**Evaluation / Implementation:**

What is your preferred design language?
- [ ] VHDL
- [ ] Verilog
- [ ] Other: ______________________________________________________________________

What is your simulation environment?
- [ ] ModelSim
- [ ] NC-Verilog
- [ ] NC-VHDL
- [ ] NC-Sim
- [ ] Verilog-XL
- [ ] Scirocco
- [ ] VCS
- [ ] VSS
- [ ] Other: ______________________________________________________________________

What is your synthesis environment?
- [ ] FPGA Express
- [ ] Leonardo Spectrum
- [ ] Synplify
- [ ] FPGA Compiler II
- [ ] BuildGates
- [ ] Design Compiler
- [ ] Other: ______________________________________________________________________

What is your Actel implementation environment?
- [ ] Libero Silver
- [ ] Libero Gold
- [ ] Libero Platinum
- [ ] Designer Gold
- [ ] Designer Platinum
- [ ] Other: ______________________________________________________________________

What is your target Actel family?
- [ ] Axcelerator
- [ ] ProASIC™
- [ ] Other: ______________________________________________________________________

**Customization / Integration:**

Do you have a design specification?
- [ ] Yes
- [ ] No

Describe your application: (attach a block diagram if possible) ______________________________________________________________________

**Line interface (front-end) information**

- What is your data rate? ______________________________________________________________________
- What is your line interface? (T1, E1, T3, E3, HSSI, SS7, etc.) __________________ How many? __________________
- Is the line interface unchannelized? ______________________________________________________________________

**HDLC Information**

- What is your total number of HDLC channels? ______________________________________________________________________
- What is your frame size? ______________________________________________________________________
- Will you be using 16-bit or 32-bit CRC? ______________________________________________________________________

**Bus Interface (back-end) Information**

- What is your bus interface? ______________________________________________________________________
- Will you need a DMA controller? ______________________________________________________________________
  - How many channels? ______________________________________________________________________
  - Is dynamic bus sizing needed?  
    - [ ] Yes
    - [ ] No
  - Is scatter-gather capability needed?  
    - [ ] Yes
    - [ ] No
- What are your interrupt requirements? ______________________________________________________________________

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To contact the local Memec distributor who sells and supports Actel, go to www.memecdesign.com/actel