**Overview**

Digital transmission systems are irreplaceable in today’s data and telecommunication networks. The Memec Design G704-E1 Framer core is a crucial building block in such systems, and is responsible for generating synchronous frame structures used at primary and secondary hierarchical levels. Specifically, the G704-E1 core works with the E1 carrier to provide a bit rate of 2048 Kbps. E1 is one of the two most widely used TDM (time division multiplexing) carriers incorporating 32 channels, each with a bandwidth of 64 Kbps.

The structural architecture of the G704-E1 core and its sophisticated interface are most beneficial when building system-on-chip solutions that demand highly specific data processing capabilities. The G704-E1 core allows users to easily combine data processing blocks with the G704-E1. The G704-E1 Framer core is fully certified by the Standard Verification Bureau.

**General Description**

The G704E1 Framer core is specifically designed to run at 2048 Kbps (E1 carrier). The main building blocks—frame synchronizer, frame analyzer, overhead handler, and frame builder—are properly partitioned, which enables devices with innovative functions to easily combine into new and competitive products.

The frame synchronizer operates in accordance with proposed Recommendation G.706, and provides information like basic frame alignment, multi-frame alignment, parallel basic frame alignment, and CRC4 calculation. In addition, the frame analyzer performs A-bit processing, includes counters that capture E-bits and CRC4 errors, and stores all received special bits in a 8x7bit register bank. The frame builder unit builds new frame and multiframe structures, and automatically computes and includes CRC4. This block does require a basic frame sync pulse since it does not incorporate an FAS synchronizer unit. The overhead handler inserts the overhead bits into the outgoing frame. Both the frame synchronizer and the frame builder output a frame reference signal, which allows them to identify each and every bit in a frame, whether the structure is basic or multiframe.

Status information for the whole core can be safely read from shadow registers, thus eliminating data changes during read-out. The complete MC-ACT-G704E1 Framer core is fully certified by the Standard Verification Bureau and has been successfully implemented by several telecommunication companies.

**Features**

- G704 framing de-framing on E1 carriers
- Basic and multiframe alignment
- Alarm bit processing
- Customizable error counters
- Selectable conditions for loss of sync
- CRC4 error checking and monitoring
- Fully synchronous

**Applications**

- Asymmetric: such as E1-ATM, Nx64-E1, E1-30BRI
- Symmetric: such as E1-E1
- Multi G704: such as E1-E2

**Target Technology**

Embedding the G704E1 Framer core in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products. The G704E1 Framer core supports many Actel devices, including:

- Axcelerator
- ProASIC™
# Questionnaire

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

## Contact Information:

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<thead>
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<th>Name:</th>
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<tr>
<td>Company:</td>
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## Pricing:

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?

- [ ] Yes
- [ ] No
- [ ] Unknown

## Evaluation / Implementation:

What is your preferred design language?

- [ ] VHDL
- [ ] Verilog
- [ ] Other: __________________________

What is your simulation environment?

- [ ] ModelSim
- [ ] NC-Verilog
- [ ] NC-VHDL
- [ ] NC-Sim
- [ ] Verilog-XL
- [ ] Scirocco
- [ ] VCS
- [ ] VSS
- [ ] Other: ____________________________

What is your synthesis environment?

- [ ] FPGA Express
- [ ] Leonardo Spectrum
- [ ] Synplify
- [ ] FPGA Compiler II
- [ ] BuildGates
- [ ] Design Compiler
- [ ] Other: ____________________________

What is your Actel implementation environment?

- [ ] Libero Silver
- [ ] Libero Gold
- [ ] Libero Platinum
- [ ] Designer Gold
- [ ] Designer Platinum
- [ ] Other: ____________________________

What is your target Actel family?

- [ ] Axcelerator
- [ ] ProASICPlus
- [ ] Other: ____________________________

## Customization / Integration:

Do you have a design specification?

- [ ] Yes
- [ ] No

Describe your application: (attach a block diagram if possible)

________________________________________________________________________

________________________________________________________________________

Why do you need a G704-E1 core?

- [ ] To replace a standard chip
- [ ] New design

What application do you plan?

- [ ] Asymmetric
- [ ] Multi G704
- [ ] Symmetric

What other blocks do you combine with the G704-E1?

- [ ] HDLC
- [ ] Slip Buffer
- [ ] UTOPIA level II Interface
- [ ] Other: ____________________________

## Other Information:

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**Corporate Headquarters:**
3721 Valley Centre Drive  
San Diego, CA 92130  
800.314.8100  
actel.info@memecdesign.com

**Regional Memec Design Contacts:**

- **Americas**
  - 3721 Valley Centre Drive  
  - San Diego, CA 92130 USA  
  - Phone: 800.752.3040  
  - Fax: 858.752.8857

- **Europe, Middle East, Africa**
  - Mattenstrasse 6a  
  - CH-5555 Brugg BE  
  - Switzerland  
  - Phone: 41.(0)32.374.32.00  
  - Fax: 41.(0)32.374.32.01

- **Asia Pacific**
  - Unit 3520, Tower 1, Metroplaza  
  - Hing Fong Rd., Kwai Fong, N.T., Hong Kong  
  - Phone: 852.2410.2720  
  - Fax: 852.2481.6937

To contact the local Memec distributor who sells and supports Actel, go to www.memecdesign.com/actel