Memec Design

DVB Modulator

Optimized for Actel

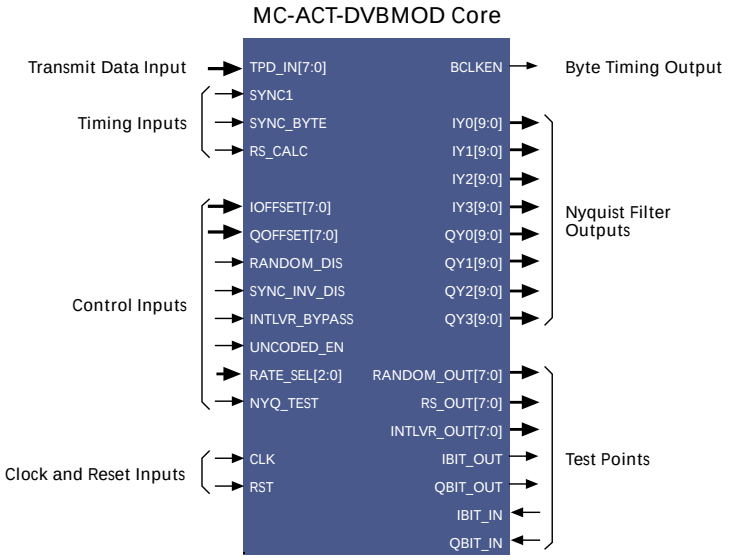
Overview

The MemecCore DVB (Digital Video Broadcasting) Modulator Core comprises a family of DVB products that comply with many transmission specifications. The cores are currently used in satellite transmission, TV cable infrastructure, and wireless terrestrial links in video and pure data applications.

Products in the DVB portfolio perform all of the digital baseband functions for the transmit side of the link, including:

- Baseband shaping
- Constellation mapping
- Convolutional interleaving
- Interpolation to the desired sampling frequency
- Randomization
- Reed-Solomon code generation
- Trellis/differential coding

The input to the core is an MPEG transport stream that uses a DVB synchronous parallel interface, as outlined in EN50083-9. The output of the core, I/Q data, is fed to DACs at the desired sampling rate.



Features

- Flexible clocking scheme
- Simpler analog reconstruction filters when a fixed frequency is used
- Data clock (DCLK) provided with transport stream
- Internal DPLL adapts the interpolation rate used for the CVI FIR filter
- The CVI FIR is a hybrid of a multiplier-free 64-polyphase FIR, combined with a linear interpolator to allow for fractional interpolation.
- Reed-Solomon coders (204,188) or (146,130); extended RS coders available
- Ramsey II or Forney convolutional interleavers with internal or external storage RAM and variable interleaving depth
- Differential coding or pragmatic trellis coding with code rates of 1/2, 2/3, 3/4, 5/6, 6/7, 7/8, 8/9, 14/15, 19/20
- Supports QPSK, 8-PSK, 16 QAM, 32 QAM, 64 QAM, 128 QAM, and 256 QAM
- Symbol rates up to 50 Msymbol/s
- Sample rates up to 200 Msample/s
- Filter scripts for quickly modifying filter roll-off and length
- Timesliced filter and digital mixers allow for multiple modulators per chip
- Coefficients reloadable on-the-fly through processor interface
- DC offset, magnitude and phase predistortion adjustable through processor interface compensate for DAC errors
- Modulation modes, filter characteristics and predistortion variables can be set through host processor interface, which can be serial peripheral interface (SPI), general host interface or RS-232

Applications

- DVB satellite modulator
- Cable head-end equipment
- LMDS/terrestrial wireless transmitter

Spec Compliance

The MemecCore DVB core family supports these specifications:

- ETSI EN300 421 (QPSK Satellite Transmission)
- ETSI EN301 210 (Digital Satellite News Gathering)
- ITU 1294 (DSS)
- EN300 429/ ITU J.83 Annex A (Digital Cable, DAVIC)
- TU J.83 Annex B (Digital Cable, DigiCipher II)

Memec Design has the building blocks and expertise to support any other modulation specs as a design requires.

Target Technology

Embedding the DVB Modulator in an FPGA provides the flexibility, upgradability, and customization benefits of programmable logic, at a cost that can be less than many application specific standard products.

The DVB core supports many Actel devices, including:

- Axcelerator

About MemecCore™ Products

MemecCore™ intellectual property (IP) cores comprise a vital element of the Memec Design portfolio. Expert designers create each core with the target silicon in mind, which ensures an optimal implementation. This practice translates into significant costs savings over comparable solutions that require more silicon and faster speed grades. Visit www.memecdesign.com/actel to review the current list of released cores and other available IP.

Actel CompanionCore

MemecCore™ Intellectual Property

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Questionnaire

Please provide Memec Design with the following information to ensure a good technical fit and the best support for your design environment. Fax the completed form to your nearest location (see below) or e-mail the information to actel.info@memecdesign.com.

Contact Information:

Name: _____ E-mail: _____

Company: _____ Phone: _____

Address: _____

City: _____ State: _____ Zip: _____ Job Title: _____

Pricing:

Do you currently purchase silicon from a Memec distributor (Impact, Insight, Unique)?

☐ Yes ☐ No ☐ Unknown

Evaluation / Implementation:

What is your preferred design language?

☐ VHDL ☐ Verilog ☐ Other: _____

What is your simulation environment?

☐ ModelSim ☐ NC-Verilog ☐ NC-VHDL ☐ NC-Sim ☐ Verilog-XL ☐ Scirocco ☐ VCS ☐ VSS ☐ Other: _____

What is your synthesis environment?

☐ FPGA Express ☐ Leonardo Spectrum ☐ Synplify ☐ FPGA Compiler II ☐ BuildGates ☐ Design Compiler ☐ Other: _____

What is your Actel implementation environment?

☐ Libero Silver ☐ Libero Gold ☐ Libero Platinum ☐ Designer Gold ☐ Designer Platinum ☐ Other: _____

What is your target Actel family?

☐ Axcelerator ☐ Other: _____

Customization / Integration:

Do you have a design specification? ☐ Yes ☐ No

Describe your application: (attach a block diagram if possible) _____

With what spec do you want to comply? (E.g. ETSI EN 301 210, ITU J.83 Annex B) _____

Which modulation modes are required? (E.g. QPSK, QAM32) _____

How many modulators per chip? (Normally 1) _____

For convolutional coders, which code rates are required? (E.g. 1/2, 2/3, 6/7) _____

Will interpolation/shaping filters be required? ☐ Yes ☐ No

If Yes, please answer the following:

What is the maximum DAC sample rate? _____

Which DAC is being used? _____ **What is its resolution?** _____

What is the interpolation rate required? _____

Does the user provide the MPEG data clock? ☐ Yes ☐ No

If the symbol rate varies, does the interpolation rate need to be continuously variable or will a limited number of fixed interpolation rates suffice?

What is the maximum symbol rate required? _____ **Is the symbol rate fixed?** ☐ Yes ☐ No

Other Information:

_____

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To contact the local Memec distributor who sells and supports Actel, go to www.memecdesign.com/actel