

INTCmodule

Description

The INTCmodule is part of Inicore's IPmodule family. This interrupt controller can be used to bundle several different interrupt sources into one main system interrupt.

The interrupt controller provides an enable register for each source request. The interrupt status register displays the current pending interrupts, the masked status register shows the status of all enabled interrupt sources. Each pending interrupt can be acknowledged individually without affecting any other interrupts. This feature helps to avoid situations where a new interrupt happens while the CPU is in the middle of the interrupt service routine.

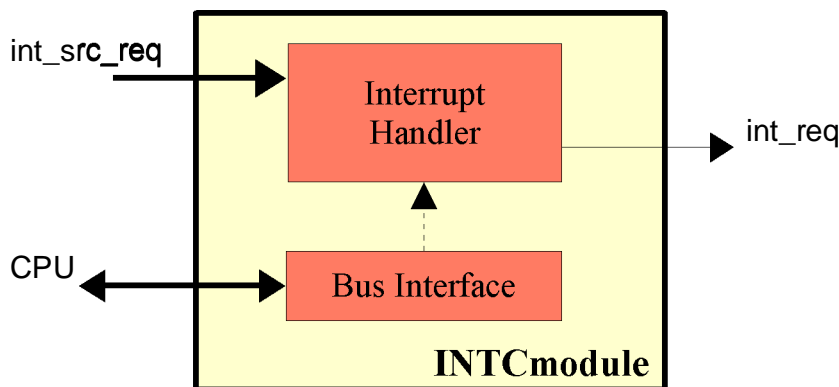


Figure 1: Block diagram

To minimize the gate count, the number of supported interrupt sources can be selected prior to synthesis.

Features

- Up to 32 different interrupt sources
- Individual interrupt acknowledgement
- Individual interrupt status register
- Masked interrupt status register
- Supports synchronous bus interfaces such as AMBA APB version 2.0
- Full synchronous design
- Synthesis options:
 - CPU readback enable
 - Number of interrupt sources

Applications

- Industrial control
- System-on-Chip
- Peripheral logic
- Embedded systems
- CPU subsystems

Utilization Table Optimized for Actel Devices

Family	Device - (speed grade)	Utilization				
		s-mod	c-mod	Tiles	RAM	Total
ProASIC ^{PLUS}	APA300			80		1%
Axcelerator	AX500-3	16	33			1%
SXA	SX32A-3	16	34			1%
eX	EX256	16	34			7%

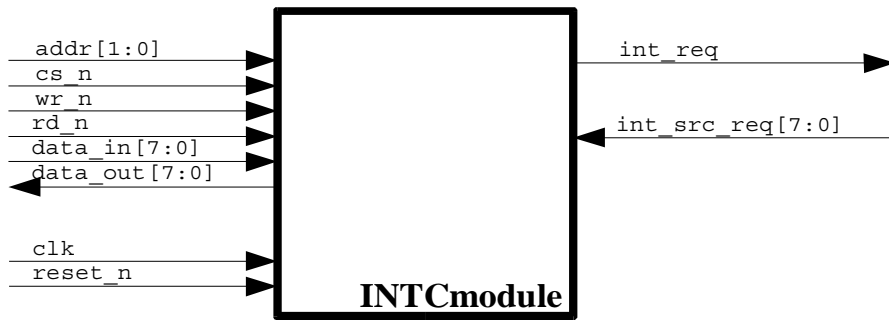


Figure 2: Symbol

Interfaces

Pin Name	Type	Description
Global Signals		
clk	in	System clock
reset_n	in	Asynchronous system reset, active low
CPU Interface		
addr[1:0]	in	Address bus input
data_in[7:0]	in	Data bus input
data_out [7:0]	out	Data bus output
cs_n	in	Module chip select, active low
rd_n	in	Active low read event
wr_n	in	Active low write event
System Port		
int_req	out	Interrupt request
int_src_req[7:0]	in	Interrupt source requests

Implementation

All IPmodule cores are designed for system integration. Standard interfaces ease connecting different cores in a system.

For gate-count optimization, the core can be configured to disable the configuration register read-back path. Synthesis options are included to use the core in 8, 16 and 32-bit systems.

With a separate APB wrapper, the core can be used in ARM subsystems.

About Inicore

- ◆ FPGA and ASIC Design
- ◆ Easy-to-use IP Cores
- ◆ System-on-Chip Solutions
- ◆ Consulting Services
- ◆ ASIC to FPGA Migration
- ◆ Obsolete ASIC Replacements

Inicore is an experienced system design house providing FPGA / ASIC and SoC design services. The company's expertise in architecture, intellectual property, methodology and tool handling provides a complete design environment that helps customers shorten their design cycle and speed time to market. Our offering covers feasibility study, concept analysis, architecture definition, code generation and implementation. When ready, we deliver you a FPGA or take your design to an ASIC provider, whatever is more suitable for your unique solution.

Deliverables

The core is available as Actel optimized netlist or as RTL version.

Actel Optimized Netlist:

- Netlist for target FPGA, EDIF, Verilog and VHDL format
- User Guide

RTL Source Code:

- VHDL or Verilog source code
- Functional verification testbench
- Synthesis script
- Timing constraints
- User guide

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