



## Introduction

The GRFPU is an IEEE-754 compliant floating-point unit, supporting both single and double precision operands. The advanced design combines high throughput with low latency, providing up to 250 MFLOPS on a 0.13  $\mu\text{m}$  ASIC process. The host interface is clean and versatile, simplifying the interfacing to processor pipelines and DSPs. The accuracy and convergence of the FPU algorithms have been proven mathematically, and the implementation has been validated with more than 20 million test vectors. Special test programs such as Testfloat, UCBTEST and IeeeCC754 have been used, as well as floating-point based application software.

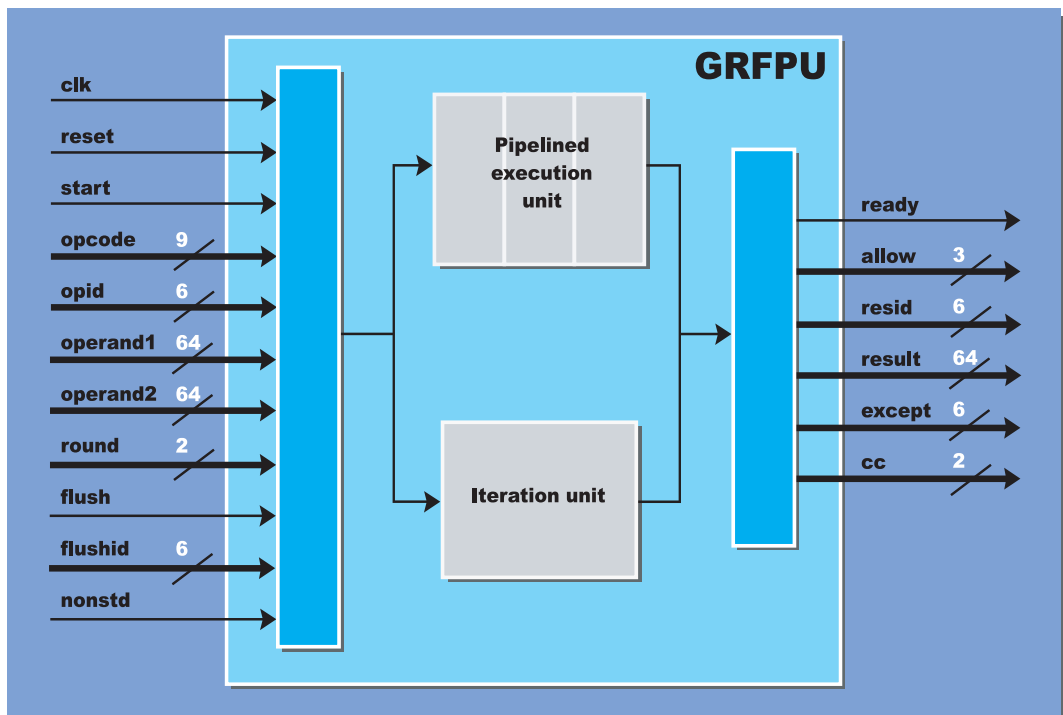


Figure 1: GRFPU block diagram

## Features

- IEEE-754 compliant, supporting all rounding modes and exceptions
- Operations: add, subtract, multiply, divide, square-root, convert, compare, move, abs, negate
- Data formats: single and double precision (32- and 64-bit floats)
- Fully pipelined, 3 clock cycles latency for all operations except divide and square-root
- Non-blocking parallel execution of divide and square-root operations
- Clean and versatile interface
- LEON FPU Control unit available
- Supports all SPARC V8 floating-point instructions
- 250 MHz (250 MFLOPS) on a typical 0.13  $\mu\text{m}$  standard cell process using less than 100 kgates
- 65 MHz (65 MFLOPS) on a Virtex-II FPGA using approximately 8,000 LUTs
- Fault-tolerant (FT) version available

## Functional Description

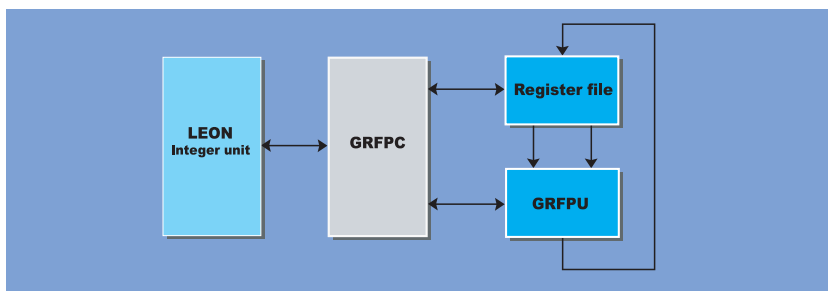
The GRFPU performs operations on single and double precision floating-point operands. All operations are IEEE-754 compliant, with exception of denormalized numbers which are flushed to zero. The specified four rounding modes and the detection of exception conditions is fully supported. An FPU operation is started by providing the operands, opcode and rounding mode on a rising clock edge. The result and the exception flags will be available three clock cycles later. The FPU is fully pipelined and a new operation can be started every clock cycle. The only exceptions are the FDIV and FSQRT instructions which require between 15 and 24 clock cycles to complete, and which are not pipelined. Instead, they are calculated in a separate non-blocking execution unit, allowing all other operations to be performed in parallel without stalling the FPU pipeline. The table below summarises the throughput and latency of the supported operations.

Operation	Throughput	Latency	Description
FADDS, FADDD, FSUBS, BSUBD, FMULS, FMULD, FSMULD	1	3	Add, subtract, multiply
FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS	1	3	Convert float/integer
FCMPS, FCMPD, FCMPE, FCMPEP	1	3	Compare
FDIVS/FDIVD	15/16	15/16	Divide (single/double)
FSQRTS/FSQRTD	23/24	23/24	Square-root (single/double)

**Table 1:** GRFPU throughput and latency

## LEON FPU Control Unit

The GRFPU can be attached to a LEON processor through the LEON FPU Control unit (GRFPC). The control unit receives SPARC FPU instructions (FPOP) from the LEON integer unit, and schedules them for execution by the FPU. The FPOPs are executed in parallel with other integer instructions, the LEON pipeline is only stalled in case of operand or resource conflicts. The control unit also includes the FPU register file, the SPARC floating-point status register (FSR) and a dual-entry deferred trap queue. The GRFPC is available for LEON2 and LEON3 both in standard version and in a fault-tolerant (FT) version.



**Figure 2:** Block diagram of a LEON processor interface

## Fault-tolerance

The fault-tolerant version of GRFPU and GRFPC includes SEU protection by design. The FPU register file is protected using (32,7) BCH coding, while all other registers are protected with TMR.

## Availability

GRFPU and GRFPC are available in netlist or VHDL source code format.

For price and licensing conditions, please contact Gaisler Research.

### CONTACT INFORMATION

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