ACTEL PCI Express Demo Board
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1 Board Layout

This is an introduction to the basic functions of the Actel PCI Express x1 Demo Board. This board provides a low-cost PCI Express solution using a TI PHY chip and an Actel ProASIC3 FPGA programmed with a Gutz Logic PCI Express x1 IP Core. This board also includes a second Actel ProASIC3 FPGA to interface with the Gutz Logic IP Standard Interface. The second FPGA allows users to develop interface designs to interface to the Gutz Logic IP without initially purchasing the IP core. Users can ‘test drive’ the IP to ensure that it meets their requirements. Once the custom design is solid, the two FPGAs designs can be merged on a custom board.

1.1 Board Components

1.1.1 TI PHY

The development board includes a XIO1100 TI PCI Express PHY. The FPGA logic of the PCI Express Physical Layer is designed to interface with this PHY chip. This PHY provides design flexibility by offering both 8-bit and 16-bit parallel interfaces based on
the PHY interface for the Intel PIPE Architecture. The Gutz Logic PCI Express x1 core uses the 16-bit option.

The XIO1100 PHY interfaces to a 2.5 Gbps PCI Express serial link with a transmit differential pair (TXP and TXN) and a receive differential pair (RXP and RXN). Incoming data at the XIO1100 PHY receive differential pair (RXP and RXN) is forwarded to the MAC on the RXDATA output bus. Data received from the MAC on the TXDATA input bus is forwarded to the XIO1100 PHY transfer differential pair (TXP and TXN).

The XIO1100 TI PHY provides many functions including the following:
- Data serialization
- Data de-serialization
- Elastic buffering
- Receiver detection
- 8b/10b encoding.

For additional information on the TI PHY, please refer to the TI specification using the following link:


1.1.2 FPGA 1

As shown in Figure 1, FPGA 1 interfaces with the TI PHY and with an IDT SRAM. It also interfaces to FPGA 2 through a standard 32-bit interface. FPGA 1 is a ProASIC3 A3P1000FG484 device. FPGA 1 includes the Gutz Logic PCI Express x1 IP core. This core is described in detail in Section 2 of this document. The Gutz Logic core provides a 16-bit Intel PIPE Spec interface to the TI PHY. PCI Express writes and reads are directed to the IDT SRAM. The IP core also allows reads and writes from FPGA 1 to PCI Express through the standard interface connected to FPGA 2. A block diagram of FPGA 1’s functionality is shown in Figure 2.
The Gutz standard interface uses separate 16-bit address and 32-bit data buses. The standard interface is very similar to an SRAM interface with read and write strobes, byte enables, and a RDY/Busy signal. FPGA 1 connects to LEDs and switches to simplify customization and debugging of the RTL code.

1.1.3 FPGA 2
FPGA 2 provides a mechanism to test the Gutz Logic PCI Express x1 IP core. This FPGA also has interfaces to an Expansion Connector and an RS232 port. Gutz Logic has developed RTL code to allow RS232 communication with FPGA 1. FPGA 1, in turn, constructs a PCI Express TLP and sends this over the PCI Express link. Figure 3 illustrates the FPGA 2 interfaces.
Figure 4 shows how this Demo board is intended to be used. The first step is development of customized logic in FPGA 2 to interface to the Gutz Logic IP core in FPGA 1, followed by testing. Once the customized logic is optimized, the two FPGAs could be merged into a single production FPGA.

1.1.4 UART/RS232 Port
The Demo Board provides an RS-232 serial port that can connect to common computer serial ports. Gutz Logic has developed UART RTL code for this interface.

1.1.5 SRAM
The Demo Board includes two IDT71V2576 128x36 SRAM devices. The SRAM interface to these devices is provided in the Gutz Logic PCI Express x1 IP core. PCI
Express reads and writes are directed to this SRAM. The IDT71V2576 specification can be downloaded from the following location:

http://www.datasheetcatalog.com/datasheets_pdf/I/D/T/7/IDT7iV2576.shtml

1.1.6 Expansion Slot
The Demo Board provides one EXP expansion connector. The EXP connector can support EXP modules. This connector allows Demo Board expansion using either one of the many off-the-shelf EXP modules or a custom-designed module. An example of a custom design would be an Ethernet EXP module that could send data to PCI Express via FPGA 2 and FPGA 1.

1.1.7 Clock and Reset Sources
The Demo Board provides reset circuitry and oscillator sockets for each of the FPGAs. The PIPE Spec interface also includes a 125 MHz clock to FPGA 1. In addition, the EXP slot has clock lines available.

1.1.8 Switches and LEDs
The Demo Board includes switches and LED circuits for debug and control of both FPGAs.
2 Gutz Logic PCI Express RTL Design

This is an introduction to the Gutz Logic PCI Express IP core. This core is developed specifically for the Actel ProASIC3 FPGA. This core takes advantage of specialized ProASIC3 design components including PLLs and internal RAM. The PCI Express core uses 53% of the VersaTiles available in an A3P1000 (the FPGA 1 device on the Demo Board).

2.1 PCI Express Layers

2.1.1 Physical Layer

The TI PHY and the FPGA PHY interface make up the Physical Layer. FPGA 1 provides all the necessary PHY functions including the following:

- Scrambling and de-scrambling of the RX and TX data
- LTSSM state machine control
- Receiving and transmitting of Link Layer Packets.

The PHY portion of the FPGA 1 code includes clock crossing to a 32-bit, 62.5 MHz domain. All other modules within the design run off the 62.5 MHz clock. This allows easier timing closure as well as simplifying place and route.

2.1.2 Data Link Layer

The Data Link Layer provides all required PCI Express DLL functions including the following:

- Transmit and receive credit calculation
- Sequence and LCRC generation and checking
- DLL error checking and generation
- Replay Buffer control for ACK/NACK processing and TLP replay
- Initial flow control
- Transmit and receive of all DLL packets

2.1.3 Transaction Layer

The Transaction Layer includes data and header queues to store nonposted, posted and completion TLPs. These TLPs, as well as messages, are decoded and processed in the transaction layer. Each TLP is checked to ensure it is not malformed. Other required TLP error checking is also provided in the Transaction Layer portion of the core.

TLPs directed to the SRAM are memory mapped through PCI Express Base Address Register (BAR) 1. The Transaction Layer portion of the core includes all required PCI Express Endpoint configuration registers. This includes a Type 0 Header as well as all required capability registers. There are also device-specific registers that can be accessed through BAR 0.

The Gutz Logic Standard Interface can access the SRAM as well as the configuration and device-specific registers. An internal arbiter controls the SRAM access. The main intent
of the Standard Interface is to allow the FPGA to master reads and writes to the PCI Express link.

For additional information on the PCI Express IP core, please refer to the Gutz Logic PCI Express x1 Core datasheet.