



## Frame Buffer Core

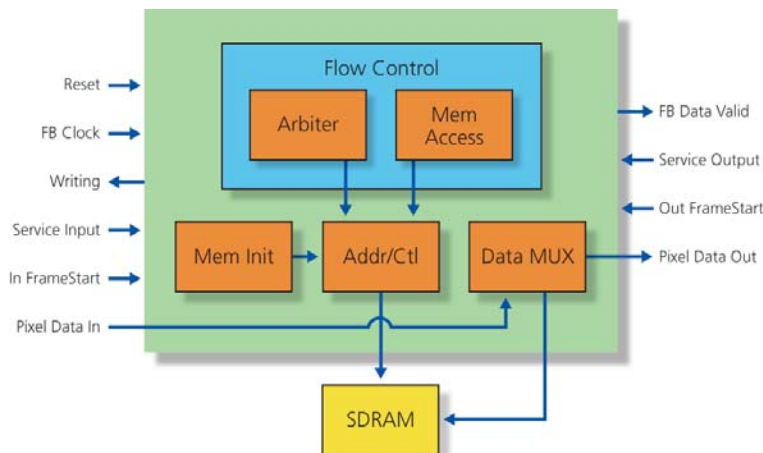


Attodyne's family of Frame Buffer (FB) cores provides functionality, which is central to most video processing applications. It facilitates the synchronization of pixel data across clock/format boundaries. Logic, external to the core, requests write and read accesses to the frame buffer. An internal arbiter determines the priority of those requests and acts accordingly. Better than 90% of the SDRAM's theoretical bandwidth is available due to the highly optimized SDRAM-access logic.

In an application, the Frame Buffer appears to be writing and reading the SDRAM simultaneously. This is achieved through the addition of small input and output FIFOs, allowing the external data to flow continuously.

Various versions of the FB core are available, depending on the application. For instance, a different FB core is required for a de-interlacing application versus a simple frame-rate converter. Please contact Attodyne and discuss your application.

### Block Diagram



## Features

### High SDRAM Bandwidth Efficiency

- Can use slower frame buffer clock
- Lower power

### Simple Interface

- Requires only a few control signals

### Data-Rate Conversion

- Frame-rate conversion
- Frame-locked
- Line-locked
- Constant In/Out pixel rate

### Uses Inexpensive SDRAM

- Lowers cost
- Large/multiple buffer instances

### Double-Buffered

- Eliminates frame tearing
- Accomplished with single SDRAM

## Applications

- In-Car Entertainment
- Medical Imaging
- Handheld devices
- Set-Top Boxes
- Notebooks
- Kiosks
- Casino Machines
- ATMs
- POS Advertising
- Avionics
- Military

The prime function of the Frame Buffer core is to facilitate the throttling of pixel data on an as-needed basis while maximizing SDRAM bandwidth. On powerup, the Mem Init module initializes the SDRAM. Once completed, control is turned over to the Flow Control module. The Arbiter is at the heart of the Flow Control module. It dictates the type of SDRAM access based on the application's set of rules. Once a decision is made, logic sets up the Mem Access module with new address coordinates and commands the SDRAM interface multiplexers to route the buses as required.

The FB is normally used with small external FIFOs (internal to the FPGA). These FIFOs permit data to move continuously across three clock boundaries, which are typically the input pixel clock, the frame buffer (SDRAM) clock, and the output (display) clock.



## Frame Buffer Core



### Device Utilization

Family	Device	Tiles	Clock Globals	I/Os	PLLs	Block RAM	Utilization
IGLOO™	AGL600	445	1	125	0	0	3.2%
ProASIC®3	A3P125	445	1	125	0	0	14.5%
Fusion	AFS250	445	1	125	0	0	7.3%

### Deliverables

- Complete IP Datasheet
- Actel Optimized Netlist
  - Netlist for target FPGA in EDIF, Verilog, or VHDL format
- RTL Source Code
  - VHDL or Verilog source code
  - Functional verification testbench
  - Complete Libero® Integrated Design Environment (IDE) project

### About Attodyne

As an Actel Solution Partner, Attodyne licenses IP cores relating to the processing, transmission, distribution, and display of video data. Attodyne's design experience and capabilities span from ultra-low noise analog circuits to 4 Gbps fiber optic communications; however, video-related FPGA work is its primary focus. In addition to licensing IP cores, Attodyne also offers reference designs, prototypes, design consultation, and product development.

Attodyne will help guide you early in your project to extract the maximum feature set that will minimize the design cost for both hardware and firmware/software. Attodyne recommends Actel's FPGAs, as Actel's Flash based FPGA architecture is uniquely suited to video/LCD applications. Actel also provides superior support and creative flexibility to match its customer's needs. Due to a close working relationship with Actel, Attodyne has extensive knowledge of its Flash FPGAs as well as Actel's roadmap. This base of knowledge is extremely important when making long-term product and manufacturing decisions.