Background

Digital Predistortion technology (DPD) enables power-efficient transmission in modern wireless communications systems. Prior to third generation (3G) cellular systems, wireless signals were relatively benign in that their envelope[1] was essentially constant. Subsequently (3G and beyond) the drive for enhanced data capacity has resulted in the wireless signal envelope becoming increasingly variable. This poses significant challenges for the transmitter and in-particular the Radio Frequency Power Amplifier (RFPA). Efficient power amplifiers tend to be non-linear, which is fine when the signal envelope is constant, however the non-linear transmission of 3G/4G signals result in the generation of troublesome interference, which can exceed regulatory requirements. To fix this there are essentially two options, but only one practical choice:

- Design a linear RFPA; such designs are expensive and highly inefficient (e.g. to transmit 20 Watts the RFPA would probably consume ~400 Watts or more). Or, more practically …
- Linearize the RFPA by a dynamic manipulation of the RFPA itself and/or its input signal. DPD is a linearization technology which enables interference-free transmission using an essentially non-linear (i.e. power efficient) RFPA.

Since 2008, drawing on 40+ years of transmitter product design expertise, Systems4Silicon has supplied, supported and evolved its DPD technology to an international customer base. The development of algorithms for DPD is a complex and costly exercise, hence the resulting solution may put significant demands upon the underlying target platform. Systems4Silicon's DPD Toolkit is scalable to optimise these demands according to the needs of the target system. It is unique to the marketplace since it is delivered as IP cores for any FPGA or ASIC.

[1] The variation of the instantaneous size of the signal as it is modulated with the digital data.

Applications

The linearization of single or multi-carrier (mixed-mode) power amplifiers for contemporary transmission standards such as 4G, 3G and DVB operating in either TDD or FDD mode. The DPD IP is not specifically configured for the transmission standard, therefore it will also operate with legacy and bespoke transmission technologies – please contact Systems4Silicon to discuss your specific requirements.

Figure 1 illustrates an example of how Systems4Silicon's DPD Toolkit may be integrated within a typical sub-system. Use of a preceding Crest Factor Reduction (CFR) block is not mandated, however it is typically employed to maximise RFPA efficiency. Systems4Silicon can supply its FlexCFR IP if required.

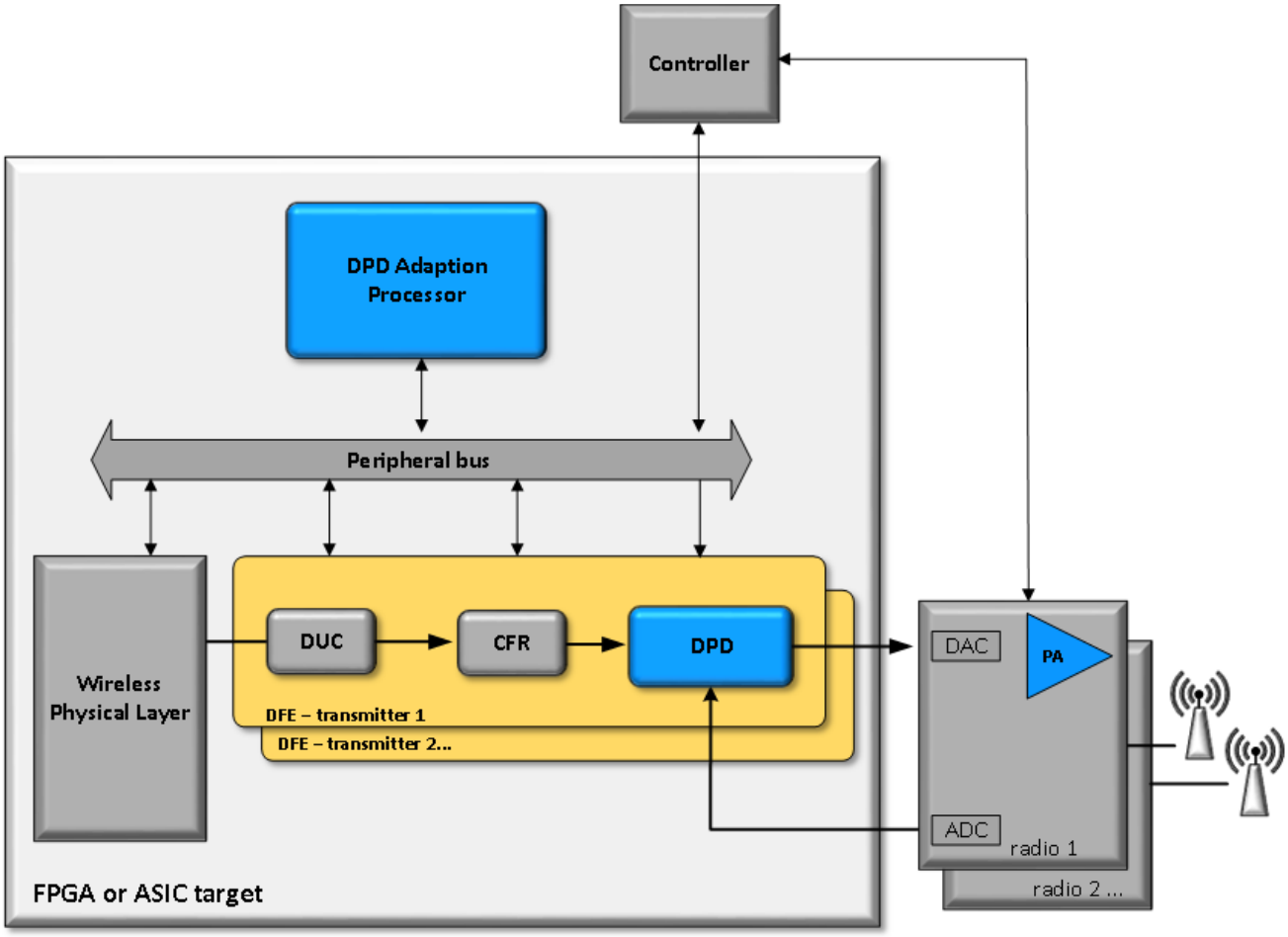

Figure 1: DPD Toolkit example sub-system architecture.

Systems4Silicon's DPD Toolkit comprises a DPD Adaption algorithm implemented in software and a DPD Core which is targeted at the real-time hardware (FPGA/ASIC).

The DPD Core includes a linear distortion compensation function for the analogue hardware. For platforms with analogue hardware that introduces low levels of linear distortion the compensation function can be omitted to minimise total resource requirements.

The DPD Adaption algorithm is coded in portable C++ for targeting at (for example) an FPGA soft-core processor, ARM Cortex hard processor or other dedicated µP/DSP. This code may be integrated with customer applications on shared processing resources or built for standalone operation. Use within an Operating System (OS/RTOS) is possible but not mandated.

Typically, a hardware platform includes a Controller unit[2] for the configuration and control of platform peripherals such as data converters, analogue gain etc. The same Controller would typically be used to manage the operation of the DPD. During operation, in addition to the linearization function the DPD Adaption processing determines other correction values required to optimise system performance, for example transmitter gain and quadrature modulator error compensation. These low-rate signals are communicated to the Controller for application to the appropriate hardware actuator in the radio.

Performance

The screenshots in Figure 2 provide an illustration of the practical performance in relation to the improvement of unwanted spectral emissions. In both cases the RFPA is Doherty architecture and the waveforms exhibit a peak to average power ratio of ~10 dB. The left-hand trace is illustrative of a mixed-mode 3G plus 4G transmission, whereas the other is representative of single carrier 4G.

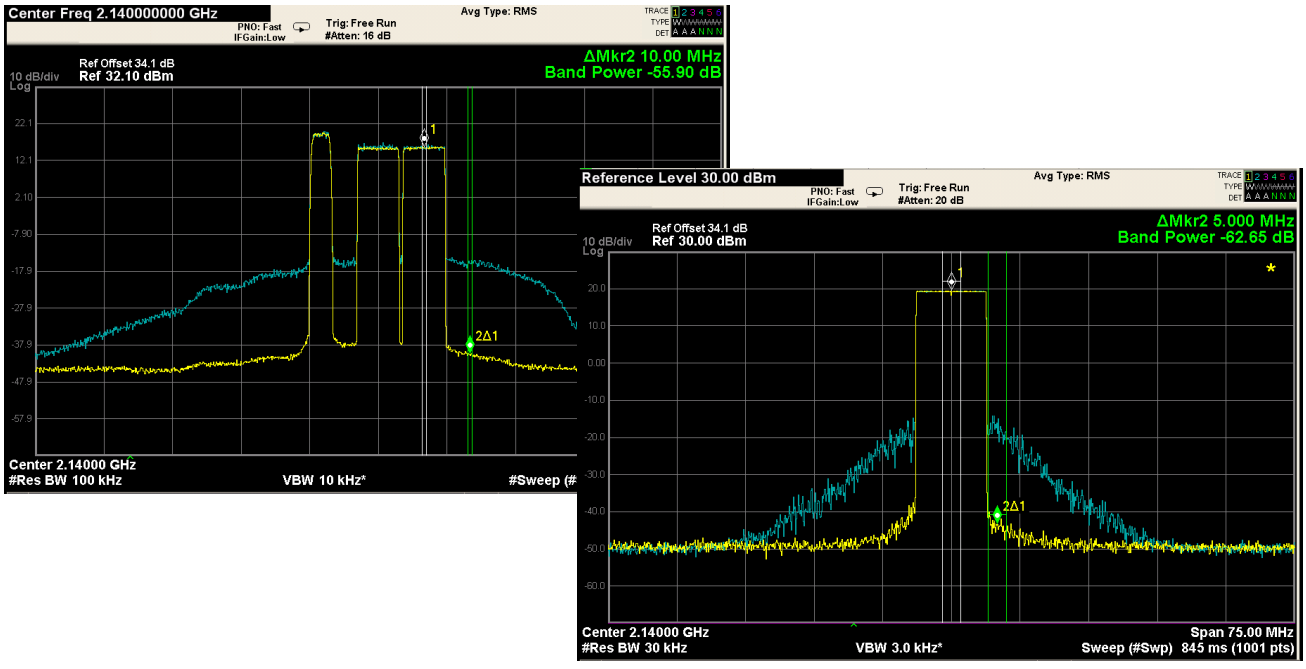

Figure 2: DPD Toolkit illustrative performance.

[2] Which could be another embedded processor.

Support

Systems4Silicon's DPD Toolkit is supplied with a comprehensive engineering data sheet and test benches. Additionally, for system integration there is a visualisation and analysis tool which provides graphical performance and behavioural metrics for the linearized transmitter system (see Figure 3). At the core of this system is a data logging facility, the file outputs of which may be analysed locally by the system integrators or delivered to Systems4Silicon thereby enabling remote support.

Furthermore, Systems4Silicon will not simply deliver the IP and wave goodbye. The DPD component is just one technology in a linearized transmitter system and within such systems, regardless of the DPD supplier, both the radio and the RFPA itself impact on the overall attainable performance. For example, the RFPA should be designed with linearization in mind and the radio bandwidth must be suitable for the anticipated linearized performance. Such design decisions and trade-offs are facilitated partly by the scalability of Systems4Silicon's DPD Toolkit solution, however, no less important than this is the detailed engineering knowledge and dedicated support that is provided by the Systems4Silicon team to help you attain the optimum performance for your system.

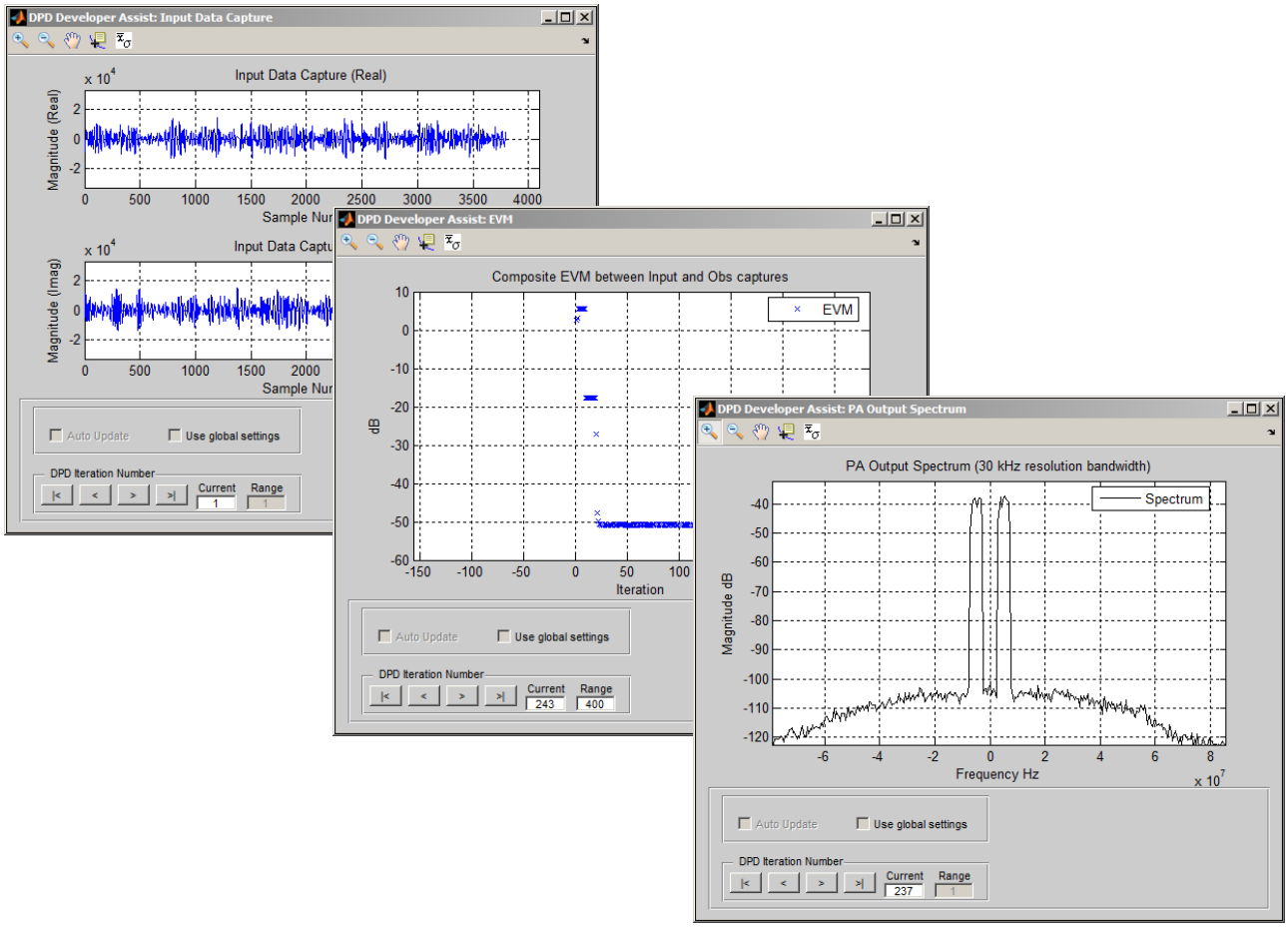

Figure 3: DPD Developer Assist integration support tool, example visualisation.

Features & Capabilities

Feature	Comment
Correction capability (non-linear)	30 dB or better ACLR improvement depending upon the DPD configuration and system specifications/characteristics.
Correction capabilities (linear)	Adaptive AQM dc-offset and imbalance correction. Adaptive gain and phase slope correction. Adaptive gain control.
Supported transmission bandwidth	Limited only by the capabilities of the FPGA/ASIC (i.e. the attainable system clock rate) and specification of the radio sub-system. State of the art with today's FPGA and data converter devices is approximately 150 MHz of modulation bandwidth.
Supported Tx channels / MIMO	Limited only by the capabilities of the FPGA/ASIC and specification of the radio sub-system. Target technology system resources may be optimised by commutating the use of the DPD's Data Acquisition sub-system and the Adaption Processor between multiple channels. The JESD204B and gigabit transceiver capabilities of today's FPGAs combined with modern converter devices mean that device pin-out restrictions are far less likely to be a limiting factor for multiple channel support.
RFPA technology	Agnostic with respect to RFPA transistor technology or RFPA topology (e.g. GaS, GaN, LDMOS, Doherty, Class A/B, Envelope Tracking, …)
Transmission standards	Agnostic with respect to transmission standard (e.g. 3G, 4G, DVB, APCO P25, BGAN and many others) and air access technique (e.g. FDD/TDD), including multi-carrier and mixed mode operation.
DPD update cycle period	Typically, better than 1.5s for a single channel system. Rapid convergence algorithms result in system ACLR typically better than 1 dB of nominal minimum within 2-3 update cycles.
Memory correction	Scalable as demanded by the RFPA characteristics.
RFPA efficiency improvement	This is not a valid metric for any DPD implementation. Typically, a RFPA will be designed to meet a particular efficiency and then the DPD enables linear behaviour at that efficiency. If, in order to meet spectral emissions, the drive to a particular RFPA has had to be reduced then the DPD will help to recover the original operating power level and hence efficiency. If the RFPA has been over-designed for the target operating power then the DPD may enable the output power and efficiency to be increased whilst maintaining linear transmission.
Convenience	In-deployment algorithmic training or calibration is not required, either at power-up or subsequently.
Crest Factor Reduction (CFR)	Crest Factor Reduction (CFR) and DPD are different yet complimentary technologies that both facilitate the enhancement of RFPA efficiency. Although often used together for optimum efficiency, this is a system design decision and not mandatory. Systems4Silicon's DPD operates with or without a preceding CFR function.

Target Device Resources

In addition to the DPD IP being scalable according to the application, the implementation is already extremely compact. Table 2 illustrates the resource utilisation for a typical implementation on Microsemi PolarFire of a single channel system that includes typical memory correction capabilities necessary for broadband operation. Table 2 illustrates the resource utilisation of a similar design on Microsemi SmartFusion2 with reduced memory correction capabilities. The SmartFusion2 ARM Cortex-M3 processor is utilised for the DPD adaption processing and is augmented by a floating-point unit supplied by Systems4Silicon as part of the DPD solution. Note that these figures are for guidance only and may vary with factors such as the specific tools settings, total device utilisation etc.

Table 1: DPD Toolkit[3] resource utilisation for Microsemi PolarFire part number MPF300T

	4LUTs	DFFs	20k LSRAM	18x18 MACC
DPD Core and Data Acquisition	4,334	5,274	38	30
Total	**299,544**	**299,544**	**952**	**924**
Utilisation	**1.45%**	**1.76%**	**3.99%**	**3.25%**

Table 2: DPD Toolkit[4] resource utilisation for Microsemi SmartFusion2 part number M2S025

	4LUTs	DFFs	18k LSRAM	18x18 MACC
DPD Core and Data Acquisition	2,722	3,395	19	16
Floating Point Unit	4,501	2,171	0	4
Total	**7,223**	**5,566**	**19**	**20**
Utilisation	**< 26.1%**	**< 20.0%**	**< 61.3%**	**< 58.8%**

Availability

Systems4Silicon's DPD Toolkit IP is immediately available for FPGA and ASIC targets together with a comprehensive Engineering Data Sheet, comprehensive test bench support and integration tools. To discuss your specific implementation requirements please contact Systems4Silicon (details below).

[3] DPD configured for a typical memory correction capability.

[4] DPD configured for reduced memory correction capability.

Contact

For information contact Richard Hewitt, Chief Technology Officer at Systems4Silicon:

UK: +44 (0)7968 162 306
Web: www.systems4silicon.com
Email: rhewitt@systems4silicon.com

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