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# Cortex-M1 v3.1 Release Notes

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This is the production release for the ARM<sup>®</sup> Cortex<sup>™</sup>-M1 IP core. These release notes describe the features and enhancements for the Cortex-M1 v3.1 core. These release notes also contain known information about system requirements, supported families, implementations, and known issues and workarounds.

## Features

The Cortex-M1 soft IP core is a member of the ARM Cortex family of processors and has been optimized for use in Actel Cortex-M1-enabled FPGAs.

## Interfaces

The main interface present on the Cortex-M1 is an AHB-Lite master interface. This can be used to connect to an AHB-Lite bus component such as CoreAHBLite, which can in turn connect to other components to build up an AMBA-based processor system. Use Actel's SmartDesign tool to create a Cortex-M1 system.

In addition to the AHB-Lite interface, Cortex-M1 also has a debug interface that is functional when you have configured the processor to include debug logic. The core also has interrupt inputs and various miscellaneous inputs and outputs.

## Delivery Types

Cortex-M1 is delivered as a core package zip (CPZ) file that can be downloaded from the web. The majority of the logic in Cortex-M1 is contained within a pre-laid-out black box macro which is tied to specific Cortex-M1 enabled FPGA devices from Actel. Some wrapper RTL code surrounds the black box. Verilog and VHDL versions of the RTL wrapper are included to allow the core to be used in either a Verilog or VHDL design flow.

## Supported Families

The following families and specific devices are supported in this version:

- IGLOO<sup>®</sup>: M1AGL250V2, M1AGL250V5, M1AGL600V2, M1AGL600V5, M1AGL1000V2, and M1AGL1000V5
- IGLOOe: M1AGLE3000V2 and M1AGLE3000V5
- ProASIC<sup>®</sup>3: M1A3P250, M1A3P400, M1A3P600, and M1A3P1000
- ProASIC3E: M1A3PE1500 and M1A3PE3000
- ProASIC3L: M1A3P600L, M1A3P1000L, and M1A3PE3000L
- Fusion: M1AFS250, M1AFS600, and M1AFS1500

## Supported Tool Flows

This version requires the following base versions of tools:

- SmartDesign
- Libero<sup>®</sup> Integrated Design Environment (IDE) v8.6 or greater

## Installation Instructions

Cortex-M1 is available through the Libero IDE IP Catalog. It can be downloaded from a remote web-based repository and installed into the user's local vault, ready for use. Once installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

## Documentation

This release contains a copy of the *Cortex-M1 Handbook* and a copy of the *Cortex-M1 Technical Reference Manual (TRM)* from ARM Ltd.

## Simulation

When a Cortex-M1 based system is generated from SmartDesign, a bus functional model (BFM) is generated for the Cortex-M1. This BFM takes the place of the black box within the Cortex-M1 during simulation. The BFM is controlled by script files (also generated by SmartDesign) and issues transfers on Cortex-M1's AHB-Lite interface to test connectivity in the system. The BFM is not a full model of the processor and cannot be used to simulate real software running on the Cortex-M1.

## Release History

Table 1 provides the release history of Cortex-M1.

Table 1 • Release History of Cortex-M1

Version	Date	Changes
3.1	September 2010	Added a more fully featured configuration of the processor for the M1A3PE1500 device. This variant of the processor is configured to include 8 KB ITCM, 4 KB DTCM, OS extensions, 16 interrupts, and the normal (3 cycle) multiplier.
3.0	May 2010	Added a more fully featured configuration of the processor for the M1AFS1500 device. This variant of the processor is configured to include 8 KB ITCM, 4 KB DTCM, OS extensions, 16 interrupts, and the normal (3 cycle) multiplier. <i>Note: If updating an instance of Cortex-M1 to v3.0 within an existing SmartDesign design, some "Error: Parameter ..." type messages will appear in the Libero IDE Log Window. These messages appear because the parameters of the core have been revised for v3.0. The messages can be safely ignored.</i>
2.7	April 2009	Removed synchronization of JTAG signals to HCLK domain. Added support for M1A3P400 and M1A3PE3000L.
2.6	January 2009	Changed to r1p0 RTL from ARM. Added support for M1AGLE3000V2, M1AGLE3000V5, M1A3P1000L.
2.5	November 2008	Added support for M1AGL1000V2, M1AGL1000V5, M1A3PE3000, M1A3P600L.
2.4	June 2008	Added support for M1AGL250V2 and M1AGL250V5.
2.3	February 2008	Added support for M1AFS1500.
2.2	December 2007	Added support for M1A3P250 and M1A3P600.

Table 1 • Release History of Cortex-M1 (continued)

Version	Date	Changes
2.1	November 2007	Added support for M1AGL600V2, M1AGL600V5, M1A3PE1500.
2.0	June 2007	Initial version, based on r0p0 RTL from ARM. Supporting M1AFS600, M1A3P1000.

## Resolved Issues in the v3.1 Release

The following issues are resolved in v3.1:

SAR 27572: Add full featured variant for M1A3PE1500 device.

## Resolved Issues in the v3.0 Release

The following issues are resolved in v3.0:

SAR 23319: Add full featured variant for M1AFS1500 device.

## Resolved Issues in the v2.7 Release

The following issues are resolved in v2.7:

SAR 13986: Wrong ARM Cortex-M1 Technical Reference Manual packaged with v2.6.

SAR 14403: Warnings in VHDL post-layout simulations.

SAR 15092: Remove unnecessary synchronization of JTAG debug signals to HCLK domain.

## Resolved Issues in the v2.6 Release

The following issues are resolved in v2.6:

SAR 12331: Update Release Note Install Instructions for all DirectCores to include Libero.

SAR 13372: Need to update power model of Cortex M1 for IGLOO and A3PL.

## Known Issues and Workarounds

Cortex-M1 v3.0 does not support the use of the Precision® synthesis tool for the VHDL flow, when targeting the M1AFS250 device; the Precision VHDL flow is supported for all other devices. The Precision Verilog flow and the Synplify® Verilog and VHDL flows are supported for all devices.



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