
CoreSDR_AHB v4.1 Release Notes

This document accompanies the production release for the CoreSDR_AHB. It describes features and enhancements of the core release and contains information about system requirements, supported families, implementations, and known problems and solutions.

Features

- High performance, single data rate controller for standard SDRAM chips, and dual in-line memory modules (DIMMs)
- Synchronous interface, fully pipelined internal architecture
- Supports up to 1024 MB of memory
- Bank management logic monitors status of up to 8 SDRAM banks
- Support for AHB bus slave interface
- Data access of 8, 16, and 32 bits are allowed by masters

Delivery Types

The CoreSDR_AHB is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with the SoC Products Group Libero[®] Integrated Design Environment (IDE). The RTL code for the core is obfuscated and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO[®]
- IGLOO[®]e
- IGLOO PLUS
- ProASIC[®]3
- ProASIC[®]3E
- ProASIC[®]3L
- SmartFusion[™]
- Microsemi Fusion[®]

Supported Tool Flows

Use Libero IDE v9.0 or later with this CoreSDR_AHB release.

Installation Instructions

Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project. Refer the Libero IDE online help for further instructions on core instantiation, licensing, and general use.

Documentation

This release contains a copy of the CoreSDR_AHB Handbook. The handbook describes the core functionality, gives implementation suggestions, and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website at www.actel.com.

Supported Test Enviroments

The following test environments are supported for CoreSDR_AHB:

- Verilog user testbench
- VHDL user test bench

Release History

Table 1 details the release history of this core.

Table 1 • CoreSDR_AHB Release History

Core Version	Date	Changes
4.1	March 2011	Fixed SAR 19346. Added support to IGLOO, IGLOOe, IGLOO PLUS and Smartfusion device family.
4.0	June 2009	Initial version

Known Issues and Workarounds

The handbook to be referred for this release is CoreSDR_AHB_HB v4.0.



Microsemi Corporate Headquarters
2381 Morse Avenue, Irvine, CA 92614
Phone: 949-221-7100 · Fax: 949-756-0308
www.microsemi.com

Microsemi Corporation (NASDAQ: MSCC) offers the industry's most comprehensive portfolio of semiconductor technology. Committed to solving the most critical system challenges, Microsemi's products include high-performance, high-reliability analog and RF devices, mixed signal integrated circuits, FPGAs and customizable SoCs, and complete subsystems. Microsemi serves leading system manufacturers around the world in the defense, security, aerospace, enterprise, commercial, and industrial markets. Learn more at www.microsemi.com.

© 2011 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.