CoreSDLC v3.0 Release Notes

This is the production release for CoreSDLC. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

The CoreSDLC macro provides a high-speed synchronous serial communication controller that utilizes the Synchronous Data Link Control (SDLC) protocol. Operation of the controller is similar to that used in the Intel 8XC152 Global Serial Channel (GSC) device working in SDLC mode under CPU control. Communication with a CPU is realized through the Advanced Peripheral Bus (APB) interface and three interrupt sources. This enables CoreSDLC to be easily interfaced with any CPU.

Key Features

- ISDN D-channel
- X.25 networks
- Frame relay networks
- Custom serial interfaces
- Based on Intel's 80C152 global serial channel working in SDLC mode
- Single and double-byte address recognition
- Address filtering enables multicast and broadcast addresses
- 16-bit (CRC-16) and 32-bit (CRC-32) frame check sequence
- NRZ and NRZI data encoding
- Automatic bit stuffing/stripping
- 3-byte deep internal receive and transmit FIFOs
- Full or half-duplex operation
- Variable baud rate
- External or internal transmit and receive clocks
- Optional preamble generation
- Programmable interframe space
- Raw transmit and receive testing modes

Supported Interfaces

CoreSDLC is available with an AMBA 3 APB slave interface.

Delivery Types

CoreSDLC is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO nano
- IGLOO PLUS
- ProASIC3E
- ProASIC®3L
- ProASIC3
- SmartFusion®
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-SU

Supported Tool Flows

CoreSDLC requires Libero IDE v8.6 or later.

Installation Instructions

The CoreSDLC CPZ file must be installed into Libero IDE. This is done automatically via the Catalog update function in Libero IDE, or the CPZ file may be manually added using the Add Core catalog feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. For RTL and obfuscated versions of the core, the FlexLM license must be installed before the core can be exported.

Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the CoreSDLC Handbook. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions. For updates and additional information about the software, devices, and hardware visit the Intellectual Property pages on the Actel website at www.actel.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have discontinued in the 3.0 release of CoreSDLC.

New Features and Devices

CoreSDLC Version 3.0 replaces the SFR interface with an APB interface.

Known Limitations and Workarounds

There are no known limitations or workarounds with the CoreSDLC v3.0 release.

Release History

Table 1 Release History

Version	Date	Changes
3.0	July 2010	Replaced SFR interface with APB interface, upper-cased top-level ports, brought out internal tdn signal, modified register map to be on 32-bit word address boundaries
2.1	January 2005	Added support for ProASIC3 and ProASIC3E devices
2.0	May 2003	Initial release

Resolved Issues in the v3.0 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CoreSDLC v3.0 release.

Table 2 Resolved Issues in the v3.0 Release

SAR	Description
11678	Bring internal signal tdn to output pin
26646	top-level ports need to be upper case to be SIPDP compliant
26647	Register map not 32-bit word aligned per SIPDP
26648	HDL module names not SIPDP compliant

Known Issues and Workarounds

No known issues have been found in the CoreSDLC v3.0 release.

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