
CoreRSENC v3.4 Release Notes

This document accompanies the production release of CoreRSENC v3.4. It describes the features and enhancements. It also contains the information on system requirements, supported families, implementations, known issues and workarounds, and resolved issues of previous version.

Features

CoreRSENC is a highly configurable core and has the following features:

- Generation of the Reed-Solomon parameterizable encoder
- Code symbol width from 3 to 8 bits
- Codeword length up to 255 symbols
- User-defined finite field primitive polynomial
- Error correction capacity up to 16 symbols
- CCSDS-16 and CCSDS-8 encoding support
- In the CCSDS mode support for data encoding presented in conventional or dual basis

Supported Interfaces

There are no standard interfaces available in the CoreRSENC core.

Delivery Types

CoreRSENC requires a register transfer level (RTL) license to be used and instantiated. Complete source code is provided for the core.

Supported Families

CoreRSENC supports the following families:

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion
- SmartFusion®
- Axcelerator®
- RTAX-S
- RTAX-D
- ProASICPLUS®
- SmartFusion®2
- IGLOO®2
- RTG4™

Supported Tool Flows

- CoreRSENC v3.4 requires Libero® software v9.0 or later
- Microsemi SoC Products Group Libero software v9.0 or higher can be used with CoreRSENC

Installation Instructions

Within the Libero SoC software, click **Add Core** in the Catalog to locate and install a local CPZ file, or use the automatic web update feature in Libero SoC. After the CPZ file is installed in the Libero SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in the Libero SoC project.

For more information about core installation, licensing, and general use, refer to the [Libero SoC Online Help](#).

Documentation

For more information about Microsemi Intellectual Property, visit: <http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>. For updates and additional information about Microsemi software, FPGAs, and hardware, visit: www.microsemi.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Release History

Table 1 shows the release history for this document.

Table 1 • Release History

| Version | Date | Changes |
|---------|---------------|--|
| 3.4 | October 2015 | The core version was updated from v3.3 to v3.4. As listed in Table 2. |
| 3.3 | April 2015 | The core version was updated from v3.2 to v3.3. |
| 3.2 | February | Added support for SmartFusion2, IGLOO2, and RTG4 families. |
| 3.1 | June 2012 | CCSDS-16 and CCSDS-8 encoding support. |
| 3.0 | February 2011 | CCSDS support, maintenance, no longer requires or support CoreConsole. |
| 2.0 | August 2007 | Initial release. |

Resolved Issues in the v3.4 Release

Table 2 shows SARs resolved in the v3.4 release of CoreRSENC.

Table 2 • Resolved SARs in CoreRSENC v3.4 Release

| SAR No. | Description |
|---------|--|
| 69802 | CoreRSENC: CCSDS-8 first root should be 120. |

Resolved Issues in the v3.3 Release

There are no resolved SARs in v3.3 release of CoreRSENC.

Resolved Issues in the v3.2 Release

There are no resolved SARs in v3.2 release of CoreRSENC.

Resolved Issues in the v3.1 Release

Table 3 shows SARs resolved in the v3.1 release of CoreRSENC.

Table 3 • Resolved SARs in CoreRSENC v3.1 Release

| SAR No. | Description |
|---------|---|
| 17224 | CCSDS support added. |
| 31715 | Handbook fix to remove incorrect CCSDS reference. |

Discontinued Features and Devices

There are no discontinued features or devices.

Known Limitations and Workarounds

No known issues have been found in the CoreRSENC v3.4 release.



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