
CorePCIF v3.6 Release Notes

This is the production release for the CorePCIF IP core. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CorePCIF is a highly configurable core, including the following features:

- Direct Master functions
- Built-in DMA controller
- Up to six configurable base address registers (BARs) plus expansion ROM support
- Supports up to six direct FIFO connections with no data loss
- Flexible backend data flow control
- Interrupt capability
- CardBus support
- Configurable user testbench
- Hot-swap extended capabilities support for compact PCI

Interfaces

CorePCIF v3.6 supports a simple synchronous backend interface, compatible with earlier versions of Actel PCI cores.

Delivery Types

The CorePCIF core is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated in CoreConsole and simulated within Actel Libero[®] Integrated Design Environment (IDE). The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Libero IDE. The RTL code for the core is obfuscated and the some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion
- IGLOO®/e
- ProASIC3L
- ProASIC® 3/E
- ProASIC^{PLUS}®
- Axcelerator®
- RTAX-S
- SX-A
- RTSX-S

Supported Tool Flows

Use Libero IDE v8.5 or later with this CorePCIF release.

Installation Instructions

The CorePCIF CCZ file must be installed into the Libero IDE. This is done automatically via the Catalog update function in Libero IDE, or the CCZ file can be manually added using the Add Core catalog feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. If a license is required, it must be installed in the Libero IDE license file.

Consult Libero IDE help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *CorePCIF Handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported:

- VHDL verification testbench
- VHDL user testbench
- Verilog user testbench

Release History

Table 1 provides the release history of the core.

Table 1 · Release History

Version	Date	Changes
3.6	April 2009	<ul style="list-style-type: none"> • Various issues resolved as listed below
3.5	November 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below • ProASIC3L support added
3.4	April 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below
3.3	March 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below
3.2	May 2007	<ul style="list-style-type: none"> • Various issues resolved as listed below • Additional parameters to allow BARs to be forced to 32-bit operation in 64-bit cores • Additional parameters to control global usage
3.1	January 2007	<ul style="list-style-type: none"> • Various issues resolved as listed below • Ability to generate the PCI clock • Ability to support an on-chip PCI arbiter and IDSEL generation
3.0	November 2006	<ul style="list-style-type: none"> • Various issues resolved as listed below • Delivery mechanism is now through CoreConsole • Support of Fusion and IGLOO families • Addition of FIFO status register to allow a host to determine how many data words are queued inside the core
2.1	February 2006	<ul style="list-style-type: none"> • Various issues resolved as listed below
2.03	February 2006	<ul style="list-style-type: none"> • Various issues resolved as listed below • CorePCIF no longer supports SX-A devices operating at 66 MHz, though 33 MHz is still supported. • Supports the Fusion family • The RAM blocks used for internal data storage can be replaced with registers for RTAX-S flows, eliminating the need to implement EDAC protection on these internal memories. • Additional parameters have been added to allow the interrupt system to be configured.
2.02	September 2005	<ul style="list-style-type: none"> • Various issues resolved as listed below
2.01	June 2005	<ul style="list-style-type: none"> • Various issues resolved as listed below
2.0	May 2005	<ul style="list-style-type: none"> • First Production release

Resolved Issues in the v3.6 Release

Table 2 lists the Software Action Requests (SARS) that were resolved in the CorePCIF v3.6 release.

Table 2 · Resolved SARs in the CorePCIF v3.6 Release

SAR	Description
14404	All families now support the USE_REGISTERS parameter, allowing logic tiles rather than RAM blocks to be used for the internal memory. The number of logic tiles used will vary based on core configuration.
14946	An additional parameter, USE_GLOBAL_CLK, has been added, which allows selection of HCLK or RCLK buffers on the clock network for AX/RTAX-S families.
14964	If a DMA transfer is terminated by the target with a target abort during the last data transfer, the core fails to set the DMA error bits in the DMA status register and retries the transfer. The core has been modified so that the DMA error bits are set and the DMA transfer is stopped.
14967	The testbench master incorrectly deasserts IRDYN during a disconnect cycle. The testbench master has been modified to deassert IRDY a cycle earlier.
13384	Verilog ProASIC3L Simulation failures (unreferenced memory module) fixed.
4888 13972 13971	Core Packaging has been updated to improve usability in SmartDesign.
15095	Handbook updates – see revision history in the handbook.
17396	Stall master functionality adjusted to allow single cycle FRAME to IRDY timing on master transfers. New STALL_MODE parameter added to enable new behavior.
17416	When STALL_MASTER is asserted and GNTN is deasserted and reasserted as the PCI master is starting the transfer, data corruption may occur. This problem has been fixed.
17665	When DMA_REG_LOC = 0, the DMA registers could still be written and read through the PCI configuration interface. The core has been updated to prevent the writes but read cycles will still return the DMA registers values.

Resolved Issues in the v3.5 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the CorePCIF v3.5 release.

Table 3 · Resolved SARs in the CorePCIF v3.5 Release

SAR	Description
74876	Utilization statistics were corrected in the handbook.
76225 77144	When using ProASIC3-based families, the internal RAM block now uses positive clock edges on both the read and write side of the RAM.
76812	When an unaligned write transfer occurs and WR_BE_RDY is asserted immediately, the core will fail to cause a “disconnect with data” on the first data transfer as required by the PCI specification. This has been fixed.
76987	The core has been modified so that the CLKBIBUF FPGA library cell is only used when the core generates the PCI clock. In other cases a CLKBUF is used.
77283	The GUI incorrectly grayed out the Use Global Resources options for TRDYN and IRDYN, based on the Master and target selections. They were swapped over. This has been fixed.
77693	The CM8DXE2 module is no longer used and has been removed.
78460	The BARn_64BIT parameters have been added into the pcicoretest Verilog module.
78461	Corrected a cell naming issue in the ram64x32.v ProASIC ^{PLUS} obfuscated file.
78605 78620 78625	Several small changes were made to the core catalogue and packaging data to correct operation in Libero IDE v8.4.
79022	When GNTN is deasserted prior to FRAMEN assertion and the core only has a single word to transfer, the core deasserts REQN. This is not a violation of the PCI specification but can cause a data starvation issue, depending on the PCI arbiter behavior. The core has been modified so REQN is not deasserted in this case.

Resolved Issues in the v3.4 Release

Table 4 lists the Software Action Requests (SARs) that were resolved in the CorePCIF v3.4 release.

Table 4 · Resolved SARs in the CorePCIF v3.4 Release

SAR	Description
75086 75725	It is possible for the DMA master to incorrectly restart a DMA read when RD_BUSY_MASTER is asserted and FIFO recovery is disabled. This can lead to the core stalling the PCI bus if the backend does not respond to the backend read request. This is corrected in this release.
75726	The del_buffer.vhd/v files have been modified to reduce the number of warnings generated by Synplicity. No functional changes have been made.

Resolved Issues in the v3.3 Release

Table 5 lists the Software Action Requests that were resolved in the CorePCIF v3.3 release.

Table 5 · Resolved SARs in the CorePCIF v3.3 Release

SAR	Description
65066 65089 68247 73988 74414	Configuration GUI updates were made so that unrequired entries are greyed out. Also various parameter rules were added.
66197 67848	Core packaging meta-data (family names) were corrected to allow cores to be correctly filtered in the IP catalogue.
71404	Compiled simulation library updates to match updated RAM cell when using Axcelerator family.
74228 74715	Documentation updates to handbook to clarify certain features. Changes are listed in the handbook revision table.
74539	When a DirectDMA master transfer is used, the core will wait for TRDY or STOP assertion before asserting IRDY. This can lead to a bus lock-up, as the master is waiting for TRDY assertion and the Target could be waiting for IRDY assertion. This problem will only occur in systems where the Target is also violating the PCI specification by not asserting TRDY or STOP. To overcome this issue, the core has been modified so that IRDY is asserted without the need for TRDY to have been asserted.

Resolved Issues in the v3.2 Release

Table 6 lists the Software Action Requests (SARs) that were resolved in the CorePCIF v3.2 release.

Table 6 · Resolved SARs in the CorePCIF v3.2 Release

SAR	Description
64831	When CoreConsole generates the top-level wrapper file, the clock port is declared as an input. From v3.1 of the core, the clock is actually a bidirectional signal.
66093	Two new parameters have been added to allow TRDY and IRDY to use either global or normal routing resources. If possible, Actel recommends that global resources be used for TRDY and IRDY.
66094	Additional generics have been added to allow individual BARs to be configured to support just 32-bit operation when the core is configured for 64-bit.
66148 66332	The core always requested 64-bit master operations when configured for 64-bit operation, irrespective of the transfer width setting in the DMA control register.
66333	Modified a sensitivity list in the config block to prevent a misleading warning during synthesis.
66372	User testbench PCI master updated to handle target not asserting ACK64N when it had asserted REQ64N.
66743	When BUSY input is held active and a master cycle is terminated prior to FRAME assertion due to GNT going away and a target access to the core backend occurs immediately, the core fails to assert STOP correctly resulting in a PCI compliance issue. The core now correctly asserts STOP under these conditions.
66744	If BUSY is asserted during a DMA master cycle, it can cause reads from the backend not to take place. The BUSY input should not affect master cycles. The core has been updated so the BUSY and ERROR inputs are ignored during master transfers as per the datasheet. This also applies to the ERROR input.

Resolved Issues in the v3.1 Release

Table 7 lists the SARs that were resolved in the CorePCIF v3.1 release.

Table 7 · Resolved SARs in the CorePCIF v3.1 Release

SAR	Description
61913	Supports on-chip arbitration. An additional generic and output has been added to allow direct connection of the core to an on-chip PCI arbiter.
61915	Allows IDSEL input to be directly driven on-chip. An additional generic has been added to allow the IDSEL input to be directly driven by an AD line.
61916	Ability to generate the PCI clock from the FPGA An additional generic and input has been added to allow the core to drive the PCI clock; that is, to act as the PCI clock source.
63287	VHDL core will not compile when DMA_REG_BAR is greater than 3. An internal range declaration only allowed DMA_REG_BAR to have values from 0 to 3. This has been corrected to allow values from 0 to 5.
63681	BAR_INITVAL should be shifted by 4 bits. The VHDL version of the core did not shift the 28-bit BAR initialization value by 4 bits to align with the BAR register bits 31:4.

Resolved Issues in the v3.0 Release

Table 8 lists the SARs that were resolved in the CorePCIF v3.0 release.

Table 8 · Resolved SARs in the CorePCIF v3.0 Release

SAR	Description
56139	If only BAR 1 is enabled, burst read cycles will fail. If BAR 0 is enabled, this problem does not occur.
57005	There is a missing include statement in the Verilog <i>coreclocks.v</i> file when using the Axcelerator family.
58586	The core should set the PCI status Master Parity Error bit only when the PCI Control Parity Error Response is set. Previous versions of the core set the Master Parity Error bit without regard to the value of the parity response bit.
58635	When configured as 64-bit, all memory BARS are also configured as 64 bits. In some cases, users may require connecting a 32-bit BAR to the core. To allow this operation, CorePCIF v3.0 includes some constants in the <i>add_phase64.vhd/v</i> files that can be modified to enforce 32-bit BAR operation.
59110	There is a missing asynchronous reset on the internal DP_END_DEL register. This may cause the synthesis tool to insert clock gating logic on the register.
60256	An additional configuration space register has been added to allow the PCI bus or the backend CPU to determine how many data words are queued inside the core when FIFO recovery mode is enabled. Refer to the latest <i>CorePCIF Handbook</i> .
60509	The latest version of Synplicity will infer RAMS when USE_REGISTERS = 1. Additional synthesis attributes were added to prevent Synplicity from inferring RAMS.
60858	Several signal/wire definitions that were not required have been removed from the RTL source code.
61218	The core was updated to avoid simultaneous read and write cycles to internal memory for ProASIC3/E, IGLOO/e, and Fusion families.

Resolved Issues in the v2.03 Release

Table 9 lists resolved SARs in the CorePCIF v2.03 release.

Table 9 · Resolved SARs in the CorePCIF v2.03 Release

SAR	Description
50085	Core should only assert SERRN when bits 6 and 8 are set in the command register.
50698	Low level ProASIC3 RTL file refers to the ProASIC3 family rather than ProASIC3E.
51106	Interrupt Modes added; INTERRUPT_MODE and REMOVED_CAPID parameters added.
51107 51108	RTL code modified to enhance logic optimization when MASTER = 0.
52308	MEM_ADD[1:0] are not driven to the correct value for a non-word-aligned I/O cycle when the unless the previous cycle was an I/O cycle.
52481	Additional comments inserted in <i>runsim.do</i> script to indicate how to add user code to the simulations
52587	The DMA control register SWFLUSH bit only flushes BAR 0.
52588	GCF/PDC/PIN files updated to handle changed bit blasted port names from Synplicity 82G.
52625	Additional parameter USE_REGISTERS added to replace internal RAMs with register arrays for RTAX-S flows.
52944	Hot-swap detection of a 33 MHz card plugged into a backplane operating at 66 MHz does not work correctly.
53334	Parity tree on the CBEN inputs was modified to avoid use of two XOR3 cells when using the RTAX-S family. This allows PCI setup times to be met with less manual intervention.

Resolved Issues in the v2.02 Release

Table 10 lists resolved SARs in the CorePCIF v2.02 release.

Table 10 · Resolved SARs in the CorePCIF v2.02 Release

SAR	Description
47729	New parameters added to allow initialization values for Command and BAR registers.
47730	New parameter added to prevent the reset network from using a global network.
47731	New top-level port added so that external circuitry can monitor the PCI Status register in the configuration space.
48504	MAST_BUSY output was not connected to the internal register; output was floating.
48724	The core mapped the Expansion ROM Configuration registers to address 28 hex instead of 3C hex. This has been corrected.
48746	The Verification testbench and core modules have been updated to increase the simulation test coverage figures. All modules now achieve 100% coverage apart from the hot-swap state machine in the <i>config.vhd</i> file.
49057 49059	User Verilog TB does not support I/O operations properly.
49141	Synplicity timing constraint files require clock reference to allow SDC constraint file to be automatically generated for Designer.
49202	Designer TCL scripts include device names with incorrect case.
49251	Designer TCL scripts use incorrect compile options for ProASIC3 and ProASIC3E families.
49500	Core does not allow I/O byte accesses to be verified and the target abort optionally generated as required by section 3.2.2.1 of the PCI specification. Core now provides lowest two bits of the PCI address on MEM_ADDR(1:0) and the CBEN values on BYTE_ENN(3:0), allowing backend logic to verify I/O access legality before asserting WR_BE_RDY or RD_STB_IN. The RD_BYTE_VALN and RD_BYTE_ENN ports have been renamed as BYTE_VALN and BYTE_ENN and contain byte information for both read and write transfers.
49502	Pcimaster module in the user verilog testbench may repeat PCI cycles.
49567	Core does not meet 66 MHz PCI timing in ProASIC3/E when Designer 62-SP2 is used. Additional placement constraints have been added to the PDC files, allowing timing to be met with Designer v6.2 SP2.
49724	Incorrect Capability ID 7 used for Vendor Capability. Core updated to use ID 9.

Resolved Issues in the v2.01 Release

Table 11 lists resolved SARs in the CorePCIF v2.01 release.

Table 11 · Resolved SARs in the CorePCIF v2.01 Release

SAR	Description
47217	Minor changes to the simulation environments to remove unnecessary warnings from the simulation logs
47244	Generics do not minimize RAM size as expected for SX-A and RTSX-S.
47247	Buffer tree on CBE updated to reduce setup delays.
47366	PCI buffering altered to increase setup margins.
47609	Added support for byte operations in the VHDL user testbench

Known Issues and Workarounds

Table 12 lists the known issues and the associated SARs.

Table 12 · Known Issues and Associated SARs

SAR	Description
61178	The core does not support 32-bit operations when in 64-bit mode. If a 32-bit cycle is carried out, the core treats it as a 64-bit operation, even though no data is provided on the upper 32 data bits. This implies that a 64-bit core should be used only in systems that are known to operate exclusively in 64-bit mode.
61204	The verification testbench includes twelve CorePCIF instantiations, along with the supporting backend logic and error injection functions. This creates a large testbench that will run slowly using the OEM version of ModelSim supplied with Libero IDE. The <i>CorePCIF Handbook</i> includes information on how to reduce simulation time.
61217	When importing the core into Libero IDE from CoreConsole, the constraints file may not be correctly installed in the Libero IDE project. The constraints files must be manually installed. In the Libero IDE file manager, right-click on the constraints section, and then import all the constraint files located in the <i>liberoproject/coreconsole/ccproject/CorePCIF/constraints</i> directory.

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