
CorePCIF_AHB v3.7 Release Notes

This is the production release for the CorePCIF_AHB IP core. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

CorePCIF_AHB is a highly configurable core, including the following features:

- Implements a PCI to AHB bridge
- Allows transfers to be initiated from the PCI or AHB side
- Supports asynchronous clocks
- Direct Master functions
- Built-in DMA controller
- Interrupt capability
- CardBus support
- Configurable user testbench
- Hot-swap extended capabilities support for compact PCI

Interfaces

The CorePCIF_AHB core supports PCI specification v2.3 and an AHB interface.

Delivery Types

The CorePCIF_AHB core is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated in CoreConsole and simulated within Microsemi SoC Products Group Libero® Integrated Design Environment (IDE). The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Libero IDE. The RTL code for the core is obfuscated and some of the testbench source files are not provided. Instead, they are precompiled into a compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.



Supported Families

- IGLOO[®]/e
- ProASIC[®]3/E/L
- ProASIC^{PLUS}[®]
- Fusion
- SmartFusion[™]

Supported Tool Flows

Use Libero IDE v9.0 or later with this CorePCIF_AHB release.

Install Instructions

The CorePCIF AHB CCZ file must be installed into Libero IDE. This is done automatically via the Catalog update function in Libero IDE, or the CCZ file can be manually added using the Add Core catalog feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. If a license is required, it must be installed in the Libero IDE license file.

Consult Libero IDE help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the CorePCIF_AHB Handbook, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Release History

Table 1 provides the release history of the core.

Table 1 Release History

Version	Date	Changes
3.7	December 2010	<ul style="list-style-type: none"> • Various issues resolved as listed below • SmartFusion support added
3.6	June 2009	<ul style="list-style-type: none"> • Various issues resolved as listed below
3.5	November 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below • ProASIC3L support added
3.4	April 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below
3.3	March 2008	<ul style="list-style-type: none"> • Various issues resolved as listed below • Additional parameters to control global usage
3.2		<ul style="list-style-type: none"> • There was no v3.2 release of CorePCIF_AHB
3.1	January 2007	<ul style="list-style-type: none"> • First Production release

Resolved Issues in the v3.7 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the CorePCIF_AHB v3.7 release.

Table 2 Resolved SARs in the v3.7 Release

SAR	Description
25204	Corrected Pin assignment in PDC constraint file.
26167	MEMORY_WIDTH parameter was changed to MEMORY_SIZE in the handbook.
27873	Resolved the read followed by write issue on the AHB bus in CorePCIF_AHB.
28199	Resolved Issue in buffer memory read/write when transferring data in the boundary offset.

Resolved Issues in the v3.6 Release

Table 3 lists the SARs that were resolved in the CorePCIF_AHB v3.6 release.

Table 3 Resolved SARs in the v3.6 Release

SAR	Description
14404	Added USE_REGISTERS parameter support for all families, allowing logic tiles rather than RAM blocks to be used for the internal memory. The number of logic tiles used is based on the core configuration.
14964	If a DMA transfer is terminated with a target abort during the last data transfer, the core fails to set the DMA error bits in the DMA status register and retries the transfer. The core has been modified to set the DMA error bits and stop the DMA transfer.
14967	The testbench master incorrectly deasserts IRDYN during a disconnect cycle. The testbench master has been modified to deassert IRDY a cycle earlier.
4888 13972 13971 11775	Core packaging has been updated to improve usability in SmartDesign.

Resolved Issues in the v3.5 Release

Table 4 lists the SARs that were resolved in the CorePCIF_AHB v3.5 release.

Table 4 Resolved SARs in the v3.5 Release

SAR	Description
76225 77144	When using ProASIC3-based families, the internal RAM block used as a data FIFO now uses positive clock edges on both the read and write side of the RAM.
76987	The core has been modified so that the CLKBIBUF FPGA library cell is only used when the core generates the PCI clock. In other cases a CLKBUF is used.
77283	The GUI incorrectly grayed out the Use Global Resources options for TRDYN and IRDYN based on the Master and target selections. They were swapped over. This has been fixed.
77693	The CM8DXE2 module is no longer used and has been removed.
78605 78620 78625	Several small changes were made to the core catalog and packaging data to correct operation in Libero IDE v8.4.
79022	When GNTN is deasserted prior to FRAMEN assertion and the core only has a single word to transfer, the core deasserts REQN. This is not a violation of the PCI specification but can cause a data starvation issue, depending on the PCI arbiter behavior. The core has been modified so REQN is not deasserted in this case.
75266	Link to datasheet in catalog display changed to link to handbook
78633	Handbook updated to clearly show BAR0 is used to access buffer memory and BAR1 the DMA control registers.

Resolved Issues in the v3.4 Release

Table 5 lists the SARs that were resolved in the CorePCIF_AHB v3.4 release.

Table 5 Resolved SARs in the v3.4 Release

SAR	Description
75086 75725	It is possible for the DMA master to incorrectly restart a DMA read when RD_BUSY_MASTER is asserted and FIFO recovery is disabled. This can lead to the core stalling the PCI bus if the backend does not respond to the backend read request. This is corrected in this release.
75726	The del_buffer.vhd/v files have been modified to reduce the number of warnings generated by Synplicity. No functional changes have been made.

Resolved Issues in the v3.3 Release

Table 6 lists the SARs that were resolved in the CorePCIF_AHB v3.3 release.

Table 6 Resolved SARs in the v3.3 Release

SAR	Description
65066 65089 68247 73988 74414	Configuration GUI updates were organized so that unnecessary entries are grayed out. Also various parameter rules were added.
66197 67848	Core packaging meta-data (family names) were corrected to allow cores to be correctly filtered in the IP catalog.
68152	Core packaging memory map information was added.
74725	Added additional generics for global reset control on TRDY and IRDY.
74994	DMA data transfers from the memory buffer will fail if the target function is disabled and memory buffer enabled. This has been fixed and the tests updated to explicitly verify the DMA transfers.

Resolved Issues in the v3.2 Release

The release following v3.1 was v3.3. There is no v3.2 Release of CorePCIF_AHB.

Resolved Issues in the v3.1 Release

This is the first production release of CorePCIF_AHB. CorePCIF_AHB allows an AHB bus system to be connected to a PCI bus. CorePCIF_AHB is built on top of the CorePCIF core. The CorePCIF release note included with this release describes the revision history for the base CorePCIF core.

Known Issues and Workarounds

Table 7 lists the known issues and the associated SARs.

Table 7 Known Issues and Associated SARs

SAR	Description
61217	When importing the core into Libero IDE, the constraints file may not be correctly installed in the Libero IDE project. The constraints files must be manually installed. In the Libero IDE file manager, right-click on the constraints section, and then import all the constraint files located in the <Libero_prj>\coreconsole\<CC_prj>\COREPCIF_AHB\constraints directory.



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