



# **CoreMemCtrl v1.3 Update for CoreMP7 Boards Using Cypress SRAM**



## Problem

The SRAM on the CoreMP7 board can be written to, but not read.

The CoreMP7 development kit board can be assembled with either GSI or Cypress SRAMs. While these devices are pin and functionally compatible, the GSI device supports a Pipeline access mode that is not supported on the Cypress device. CoreMemCtrl was originally developed with the GSI part using the Pipeline mode, and it was only later discovered that the Cypress device only supported the Flow-Through mode.

The problem manifests itself when reading the SRAM on the board. With CoreMemCtrl v1.2 and a Cypress device, the SRAM can be written to, but it cannot be read. This was discovered after a large number of CoreMP7 boards had been built with the Cypress device, so it is no longer possible to fix the problem by only building the boards with the GSI part.

## Solution

The solution is to update CoreMemCtrl to support both Pipeline and Flow-Through modes, which has already been implemented. The new CoreMemCtrl v1.3 (included in the IP vault in CoreConsole v1.3 and later) adds a Synchronous SRAM mode configuration option that was not present in CoreMemCtrl v1.2. The Synchronous SRAM mode configuration options are Pipeline or Flow-Through, and the appropriate option will depend on the target board and the SRAM parts used.

## Implementation

CoreMemCtrl v1.3 is designed to connect to synchronous SRAMs that exhibit either pipeline or Flow-Through read behavior. The output data from the synchronous SRAM is assumed to be valid just after the SRAM clock edge that follows the edge on which the read address is clocked into the SRAM in Pipeline mode. In Flow-Through mode, an additional register is implemented in the FPGA to accomplish the same condition. CoreMemCtrl has been used with the GS88018 synchronous SRAM device from GSI Technology in Pipeline mode, with the following static values applied to certain device inputs: FTn = 1, LBO<sub>n</sub> = 1, E2 = 1, GW<sub>n</sub> = 1, ZZ = 0, ADSP<sub>n</sub> = 1, ADSC<sub>n</sub> = 0, ADV<sub>n</sub> = 1. CoreMemCtrl has also been used with the CY7C1363 synchronous Flow-Through SRAM device from Cypress, with the following static values applied to certain device inputs: MODE = 1, CE2 = 1, GW<sub>n</sub> = 1, ZZ = 0, ADSP<sub>n</sub> = 1, ADSC<sub>n</sub> = 0, and ADV<sub>n</sub> = 1.

For the Cypress memories on a CoreMP7 board, users need to use Flow-Through mode. For GSI memories on a CoreMP7 board, users need to use either Pipeline or Flow-Through mode. For the GSI memories, the board has a jumper (JP48) that selects Pipeline or Flow-Through mode: when the jumper is not selected, the mode is set to Pipeline; when the jumper is selected, the mode is set to Flow-Through.

Users experiencing problems writing to SRAM should check to see if Cypress memories are installed on the board. The SRAM memories are assembled on the back of the board (devices U6 and U8). If Cypress memories are installed, the updated CoreMemCtrl v1.3 must be used and Flow-Through mode selected in the CoreMemCtrl configuration dialog in CoreConsole.

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