CoreMBX v2.0 Release Notes

This is the production release for the CoreMBX IP core. These release notes describe the features and enhancements for CoreMBX v2.0. These release notes also contain known information about system requirements, supported families, implementations, and known issues and workarounds.

Features

- Mailbox simultaneously accessible from an AMBA advanced high-performance bus (AHB)/AHB-Lite master and an advanced peripheral bus (APB) master
- Mailbox memory storage elements made of either dual-port SRAM or FIFO blocks
- INIT/CONFIG master interface suitable for initializing CoreABC via AHB-Lite master
- Configurable number of interrupt flags between two processors
- Optional ROM built of FPGA tiles for up to 40 ROM words

Interfaces

CoreMBX has one AMBA AHB/AHB-Lite slave interface and one APB slave interface.

Delivery Types

CoreMBX is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole or SmartDesign. Simulation, synthesis, and layout can be performed with Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated and some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

The following families and specific devices are supported in this version:

- Fusion®
- ProASIC®3
- ProASIC3E
- ProASIC3L
- IGLOO®
- IGLOOe

Supported Tool Flows

This version requires the following base versions of tools:

- Libero IDE v8.4 or higher
- CoreConsole v1.4 (optional)

Install Instructions

The CoreMBX CCZ file must be installed using either the CoreConsole IDP or Libero IDE.

CoreConsole Instructions

Close all CoreConsole projects and use **Actions > Add** to database in CoreConsole to locate and install a local CCZ file, or use the automatic web update feature in CoreConsole. Once the CCZ file is installed in CoreConsole, the core can be instantiated, configured, and exported to the Libero IDE environment.

For the RTL release version of the core, the FlexLM license must be installed and Libero IDE restarted before the core can be configured and generated within CoreConsole . Refer to the Libero IDE online help for instructions about core installation and licensing.

Libero IDE/SmartDesign Instructions

Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

For the RTL release version of the core, the FlexLM license must be installed and Libero IDE restarted before the core can be configured and generated within SmartDesign. Refer to the Libero IDE online help for instructions about core installation and licensing

Documentation

This release contains a copy of the CoreMBX Handbook, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions. If using CoreConsole, the documentation can be viewed by right-clicking the Core Selection window in CoreConsole after the core has been installed. If using SmartDesign, refer to the Libero oIDE nline help for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, please visit the Intellectual Property pages on the Actel web site at www.actel.com.

Supported Test Environments

This version supports the following environments:

- Verilog user testbench
- VHDL user testbench

Discontinued Features and Devices

No features have been discontinued in the CoreMBX v2.0 release.

Resolved Issues in the CoreMBX v2.0 Release

There are no resolved issues in the CoreMBX v2.0 release; this is the first production release of CoreMBX.

Known Limitations and Workarounds

Decimal Numbers

In this release of CoreMBX, if using the ROM configuration in the CoreConsole or SmartDesign IP configurator GUI, you will need to enter all numbers in decimal notation for the ROM address/data pair fields.

Stitching

If using the Auto Stitch feature in CoreConsole, some connections may not occur as expected. When using CoreConsole, Actel recommends that you perform manual stitching. If you must use Auto Stitch, Actel recommends that you do the following:

1. Instantiate your first processor and bus interface (e.g., Cortex-M1 and CoreAhbLite) along with CoreMBX.
2. Click **Actions > Auto Stitch** and check that the connections in the Auto Stitching pop-up configuration GUI match your required connections, or make changes as necessary to meet your requirements. Then press **Stitch**.
3. Instantiate your second processor and bus interface (e.g., CoreABC and CoreAPB).
4. Click **Actions > Auto Stitch** and check that the connections in the Auto Stitching pop-up configuration GUI match your required connections, or make changes as necessary to meet your requirements. Then press **Stitch**.
5. Add any other peripherals to either bus interface and continue to build your system.

In CoreConsole, if trying to connect the Init/Config master bus interface of CoreMBX to the Init/Config slave bus interface of CoreABC, you may encounter issues that can be worked around in the following manner, using Auto Stitch To Top Level:

1. Click **Actions > Auto Stitch To Top Level**. Click the CoreMBX instance and make sure the InitCfg_bif bus is checked, along with any other ports of the CoreMBX instance that you wish to bring to the top level of the CoreConsole design. Then press **Stitch**.
2. With the Auto Stitch to Top Level pop-up configuration GUI still open, click the CoreABC component instance and make sure that the InitConfig bus is checked, along with any other port of the CoreABC instance that you wish to bring to the top level of the CoreConsole design. Then press **Stitch**. Press **OK** to close the pop-up configuration GUI window.
3. Generate the CoreConsole design and connect the appropriate InitCfg_bif_* outputs from CoreMBX to the appropriate InitConfig_* inputs of CoreABC in SmartDesign, or your own custom HDL in which the CoreConsole subsystem is instantiated.

In SmartDesign, if trying to connect the Init/Config master bus interface of CoreMBX to the Init/Config slave bus interface of CoreABC, you may encounter issues that can be worked around in the following manner, after performing the Auto Connect action within the SmartDesign canvas:

- Within the SmartDesign grid, make connections between the INIT* outputs of the CoreMBX instance to the INIT* inputs of the CoreABC instance. Refer to the Libero IDE online help for details on making connections in the SmartDesign GUI.

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