

CoreFIR v7.0 Release Notes

Introduction

This document accompanies the production release for CoreFIR. It describes features and enhancements of the core release and contains information about system requirements, supported families, implementations, and known limitations and workarounds. CoreFIR is optimized for use with Microsemi SoC Products Group RTAX™-DSP devices, making use of on-chip multiplier-accumulator blocks.

Features

- Highly configurable DirectCore RTL generator
- Choice available between fully Enumerated single rate, Folded single rate FIR, Multi-rate interpolation, and Multi-rate decimation implementations.
- Supports FIR filters of 2 up to 1024 taps
- 2 to 18-bit input data precision
- 2 to 18-bit coefficient precision
- Signed or unsigned data and coefficients
- Full precision output
- Coefficient symmetry optimization
- Run-time reloadable coefficients, multiple coefficient sets, or fixed coefficients.

Interfaces

There is no standard AMBA interface available.

Delivery Types

The CoreFIR requires an RTL license to be used and instantiated. Complete source code is provided for the core.

Supported Families

RTAX-DSP (Axcelerator RTAX2000D, Axcelerator RTAX4000D)

Supported Tool Flows

- Use SoC Products Group Libero® Integrated Design Environment (IDE), v9.1 or higher
- Supports only Windows operating systems

Installation Instructions

Use Libero IDE to install the CoreFIR CPZ. Within Libero IDE, click the **Add Core** button in the Catalog window to locate and install a local CPZ file, or use the automatic web update feature in Libero IDE. Once the CPZ file is installed in Libero IDE, the core can be configured, generated, and instantiated within SmartDesign for inclusion in your Libero IDE project.

Documentation

- The release contains a copy of the [CoreFIR v7.0 Handbook](#). Refer to the Libero IDE online help for instructions on obtaining IP documentation.
- For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the SoC Products Group website, www.actel.com.

Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

Release History

Table 1 Release History

Version	Date	Changes
7.0	March 2011	Decimation filter option added.
6.0	December 2010	Folded single-rate FIR and Polyphase interpolation filter options added.
4.1	July 2010	Improved filter throughput. The 4.1 release supports RTAX-DSP family only.
4.0	August 2009	Fully enumerated MAC-based FIR filter implementation. The release supports RTAX-DSP family only.
3.0	May 2006	Constant Coefficient Algorithm implemented.
2.0	January 2005	First production release.

Resolved Issues in the v7.0 Release

Table 1 Resolved SARs in CoreFIR v7.0 Release

SAR	Description
30457	Decimation architecture is not supported in CoreFIR 6.0.
30300	Minimum Libero version should be 9.1, however, it is specified to be 8.6.
30458	TGI-interpolation filter should be seen as 'Multi-rate'.

Resolved Issues in the v6.0 Release

Table 2 Resolved SARs in CoreFIR v6.0 Release

SAR	Description
28646	Implement semi-parallel (folding) filter type.
29750	CoreFIR v4.1 does not support up-sampling/interpolation architecture.

Resolved Issues in the v4.1 Release

Table 3 Resolved SARs in CoreFIR v4.1 Release

SAR	Description
20214	Implement RTL licensing.
20420	Correct typos on the handbook.
26463	Eliminate extended datapath delays by inserting extra pipeline registers.
26466	Double register high fanout signals to support synthesis replication feature.

Resolved Issues in the v4.0 Release

No issues resolved. This was the first release of the MAC-based FIR filter.

Resolved Issues in the v3.0 Release

No issues resolved. The Constant Coefficient architecture was added.

Known Limitations, Issues, and Workarounds

When there is no valid license installed but a user attempts to instantiate the core, the user interface isn't accessible. To access the user interface install the valid RTL license.



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