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# CoreFFT v5.0 Release Notes

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## Introduction

This document accompanies the production release for CoreFFT. It describes features and enhancements of the core release and contains information about system requirements, supported families, implementations, and known limitations and workarounds. CoreFFT is optimized for use with Microsemi SoC Product Group RTAX-DSP family of FPGA devices, making use of on-chip multiplier-accumulator hard macros.

## Features

- Highly configurable DirectCore RTL generator
- Choice of Radix-2 In-place architecture or Radix-22 Streaming FFT
- Forward and inverse complex Fast Fourier Transform (FFT)
- Transform sizes: 32-, 64-, 128-, 256-, 512-, 1024-, 2048-, 4096-, and 8192-point (In-place architecture), 16-, 32-, 64-, 128-, 256-, 512-, and 1024-point (Streaming architecture)
- 8- to 32-bits I/O real and imaginary data and twiddle coefficients
- Two's complementary I/O data
- Natural input and output sample order
- Selection of conditional or unconditional block floating point scaling (In-place architecture), pre-defined scaling schedule (Streaming architecture)
- Embedded RAM-block based twiddle look-up table (LUT)
- Built-in memory buffers
- Handshake signals to facilitate easy interface to the user circuitry

## Interfaces

There is no standard AMBA interface available.

## Delivery Types

The CoreFFT requires an RTL license to be used and instantiated. Complete source code is provided for the core.

## Supported Families

RTAX-DSP (Axcelerator RTAX2000D, Axcelerator RTAX4000D)

## Supported Tool Flows

- Use SoC Products Group Libero® Integrated Design Environment (IDE), v9.1 or higher
- Only Windows operating systems are supported

## Installation Instructions

Use Libero IDE to install the CoreFFT CPZ. Within Libero IDE, click the Add Core button in the Catalog window to locate and install a local CPZ file, or use the automatic web update feature in Libero IDE. Once the CPZ file is installed in Libero IDE, the core can be configured, generated, and instantiated within SmartDesign for inclusion in your Libero IDE project.

## Documentation

- This release contains a copy of the [CoreFFT v5.0 Handbook](#). Refer to the Libero IDE online help for instructions on obtaining IP documentation.
- For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website, [www.actel.com](http://www.actel.com).

## Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

## Discontinued Features and Devices

There are no discontinued features or devices.

## Release History

**Table 1** Release History

Version	Date	Changes
5.0	May 2011	Streaming FFT architecture is added. The 5.0 release supports RTAX-DSP family only
4.0	May 2010	As listed in the Table 3 below. The 4.0 release supports RTAX-DSP family only
3.0	May 2007	Configurable 8- to 16-bit data precision
2.0	September 2005	First production release

## Resolved Issues in the v5.0 Release

**Table 2** Resolved SARs in CoreFFT v5.0 Release

SAR	Description
32053	Add Streaming architecture to transform high rate signals

## Resolved Issues in the v4.0 Release

**Table 3** Resolved SARs in CoreFFT v4.0 Release

SAR	Description
11570	Eliminate module names reserved by Libero IDE for other purposes
11732	Resolve the core installation issues
13857	Indicate in documentation the core output latency

## Known Limitations and Workarounds

Multiple instances of the FFT aren't supported on a single Libero IDE project. In order to instantiate multiple FFT instances, RTL code of each instance needs to be manually modified by changing modules/entities names to be unique.



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