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CoreCortexM1 v3.0 Release Notes

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About Microsemi

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Updated changes related to CoreCortexM1 v3.0.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreCortexM1 v2.0.

Contents

2 CoreCortexM1 v3.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreCortexM1 v3.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

The CoreCortexM1 soft IP core is a member of the ARM Cortex family of processors and has been optimized for use in Microsemi PolarFire FPGAs.

2.3 Interfaces

The CoreCortexM1 is supplied with an AMBA AHB interface.

2.4 Delivery Types

CoreCortexM1 is available for free, but the user needs to fill up the license agreement with Microsemi.

2.5 Supported Families

- PolarFire

2.6 Supported Tool Flows

- CoreCortexM1 requires Libero® System-on-Chip (SoC) software v12.100 or later.
- Microsemi® SoC Products Group Libero software v12.100 can be used with CoreCortexM1.

2.7 Installation Instructions

The CoreCortexM1 CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreCortexM1 Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

CoreCortexM1 v3.0 supports Bus Function Model (BFM) based testbench.

2.10 Resolved History

This is the initial version of the CoreCortexM1. There are no unresolved issues in the v3.0 release.

2.11 Discontinued Features and Devices

This is the initial version of the CoreCortexM1. Hence, there are no discontinued features or devices.

2.12 Known Limitations and Workarounds

This is the initial version of the CoreCortexM1. Hence, there are no known limitations and workarounds.