
CoreCORDIC v3.0 Release Notes

Introduction

This is the production release for CoreCORDIC. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known limitations and workarounds.

Features

Intended Use

CoreCORDIC is an Actel FPGA-optimized CORDIC engine (Coordinate Rotation Digital Computer Rotator Function). Depending on the configuration defined by the user, the resulting module implements pipelined-parallel, word-serial, or bit-serial architecture in one of two major modes: rotation or vectoring.

Key Features

The key features of CoreCORDIC are:

- Vector rotation – Conversion of polar coordinates to rectangular coordinates
- Vector translation – Conversion of rectangular coordinates to polar coordinates
- Sine and cosine calculation
- Vector (X, Y) magnitude and phase ($\arctan[X/Y]$) calculation
- 8-bit to 48-bit configurable word size
- 8 to 48 configurable number of iterations
- Parallel pipelined architecture for the fastest calculation
- Bit-serial architecture for the smallest area
- Word-serial architecture for moderate speed and area
- Word parallel data I/Os

Delivery Types

CoreCORDIC is only licensed using RTL.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO[®]
- IGLOOe
- IGLOO PLUS
- ProASIC3

- ProASIC3E
- ProASIC3L
- SmartFusion
- Fusion
- ProASIC^{PLUS}[®]
- Axcelerator[®]
- RTAX-S
- RTAX-DSP
- SX-A
- RTSX-S

Supported Tool Flows

CoreCORDIC requires Actel Libero IDE v8.6 or later.

Installation Instructions

The CoreCORDIC CCZ file must be installed into Libero IDE. This is done automatically via the Catalog update function in Libero IDE. Alternatively, the CCZ file may be manually added using the **Add Core** catalog feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. The FlexLM license must be installed before the core can be exported.

Refer to the Libero IDE online help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *CoreCORDIC Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions. For updates and additional information about the software, devices, and hardware visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

This version supports the following test environments:

- VHDL user testbench: Rotation Mode
- VHDL user testbench: Vector Mode
- Verilog user testbench: Rotation Mode
- Verilog user testbench: Vector Mode

Discontinued Features and Devices

No features or devices have been discontinued in this release.

New Features and Devices

No new features or devices have been added in this release.

Release History

Table 1 CoreCORDIC Release History

Version	Date	Changes
3.0	May 2010	Packaged core and made numerous fixes. Refer to table 2 for details
2.0	April 2006	Initial version of this core

Resolved Issues in the v3.0 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the v3.0 release of CoreCORDIC.

Table 2 Resolved SARs in CoreCORDIC v3.0 Release

SAR	Description
13497	Generated core does not seem to match up with the datasheet pin description
19458	CoreCORDIC for Verilog requires Package Directory
19459	Remove package directory dependency for VHDL
20132	CoreCORDIC in Word Serial mode has RTL and document mismatches

Known Limitations in the v3.0 Release

There are no known limitations.



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