CoreCIC v2.0 Release Notes

This document accompanies the production release of CoreCIC v2.0 IP core. It also contains the information on the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

Key Features

CoreCIC has the following key features:

- Fixed or programmable rate change from 2 to 1024
- One to eight integrator-comb stages
- Comb differential delay of one or two
- Signed 2's complement input data
- Input data width from 1 to 32 bits
- Output data width up to 100 bits
- Choice of output data truncation and two rounding types
- Optional Hogenauer pruning
- Support for up to 64 channels

Supported Interface

No standard interface is available.

Delivery Types

CoreCIC is distributed with Libero® System-on-Chip (SoC) design software. The complete hardware description language (HDL) source code is provided for the core and testbenches.

Supported Families

CoreCIC supports the following families:

- SmartFusion®2
- IGLOO®2
- RTG4

Supported Tool Flows

CoreCIC supports the following tool flows:

- CoreCIC v2.0 requires Libero v11.3 or later
- Supports Windows and Linux operating systems

Installation Instructions

The CoreCIC CPZ file must be installed into the Libero SoC software. This is done automatically through the **Catalog update** function in the Libero software, or the CPZ file can be added using the **Add Core Catalog** feature, manually. Once installed in the Libero SoC Catalog, the core can be instantiated and configured. Refer to the Libero SoC User Guide instructions on core installation and licensing.

Documentation

This release contains a copy of the CoreCIC Handbook, which describes the core functionality, step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and suggestions for implementation.

For updates and additional information about the software, devices, and hardware, refer to the Intellectual Property pages on the Microsemi web site.

Supported Test Environments

CoreCIC supports the following test environments:

- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

This is the first production release of CoreCIC v2.0.

Known Limitations and Workarounds

There are no known limitations or workarounds.

Release History

Table 1 shows the release history of CoreCIC.

Table 1 Release History

Version	Date	Changes
2.0	August 2014	Initial release

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