
CoreCFI v2.0 Release Notes

This is the production release for the CoreCFI IP core. These release notes describe the features and enhancements of the core. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

The CoreCFI design is primarily a state machine that controls the interfaces to the Fusion Flash memory and the external CFI interface. CoreCFI implements a subset of the Common Flash Memory Interface Specification Release 2.0. Some of the key features of CoreCFI are as follows:

- Support for CFI commands:
 - Read Query
 - Read ID Codes
 - Read Array
 - Read Status
 - Clear Status
 - Erase Page
 - Single Write
 - Multi-Write
 - Page Lock
 - Page Unlock
- Variable Flash memory access size (controlled by CoreCFI generic)
- 128-byte Write page buffer and Write/Erase size
- 16-byte page Read buffer
- 8-bit, 16-bit, and 32-bit operation

Interfaces

CoreCFI supports the standard Flash memory device interface (Common Flash Interface). For more information, refer to a datasheet for a generic Flash chip, such as a Micron MT28F320J3. CoreCFI also has a Fusion Flash memory interface for access to the Actel Fusion™ nonvolatile memory (NVM).

Delivery Types

The CoreCFI core is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

The Evaluation version allows simulation of CoreCFI using ModelSim® or Actel Libero® Integrated Design Environment (IDE).

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Actel Libero IDE. The RTL code for the core is obfuscated, and some of the testbench source files are not provided.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion

Supported Tool Flows

Use CoreConsole v1.2.1 and Libero IDE v7.3 or later with this CoreCFI release.

Installation Instructions

The CoreCFI CCZ file must be installed using CoreConsole. Using **Actions > Add to database** in CoreConsole, locate and install the CCZ file. Then shut down and restart CoreConsole (this should be done when no CoreConsole project is open). Once installed in CoreConsole, the core can be instantiated, configured, and exported to Libero IDE. For the RTL and Obfuscated versions of the core, the FlexLM license must be installed and CoreConsole restarted before the core can be exported. Consult CoreConsole online help for further instructions with core installation and licensing.

Documentation

This release contains a copy of the *CoreCFI Handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and includes implementation suggestions. The documentation can be viewed by right-clicking the Core Selection pane in CoreConsole after the core has been installed. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported for CoreCFI:

- VHDL user testbench
- Verilog user testbench
- VHDL full verification testbench

Known Issues and Workarounds

There are no known issues for this release of the CoreCFI (v2.0).

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