
CoreAhbSram v1.4 Release Notes

This is the production release for the CoreAhbSram v1.4 IP core. These release notes describe the features and enhancements for CoreAhbSram. These release notes also contain known information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Intended Use

CoreAhbSram provides an AMBA advanced high-performance bus (AHB) interface to the embedded SRAM blocks within Fusion, IGLOO[®], and ProASIC3[®]E families of devices. AHB masters read from and write to the memory resources of the SRAM blocks through the AHB Slave interface of CoreAhbSram.

Key Features

- Provides standard AHB slave interface
- 32-bit data interface
- Supports byte, halfword, and word (32 bit) access to SRAM
- Ability to logically merge multiple SRAM blocks into one large area of SRAM
- Size of SRAM is configurable from 2048 bytes to 32768 bytes, in steps of 2048 bytes

Interfaces

CoreAhbSram contains an AMBA advanced high-performance bus (AHB) Slave interface to connect to AMBA-based systems.

Documentation

This release contains a copy of the [CoreAhbSram](#) datasheet. The CoreAhbSram datasheet describes the core functionality.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at www.actel.com.

Delivery Types

CoreAhbSram is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero[®] Integrated Design Software (IDE). The RTL code for the core is obfuscated.

This core is licensed as part of the default Libero IDE license set and no additional license is required

RTL

Complete RTL source code is provided for the core.

Supported Families

This version of the core supports the following families of devices:

- Fusion
- IGLOO, IGLOOe, and IGLOO PLUS
- ProASIC3, ProASIC3E, and ProASIC3L

Supported Tool Flows

This version of the core requires the following tool:

- Libero IDE v8.4 SP1 or later.

Installation Instructions

The CoreAhbSram CCZ file must be installed into Libero IDE. Within Libero IDE, click the **Add Core** button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

Consult the Libero IDE online help for instructions on core installation and licensing.

Release History

Table 1 provides the release history of CoreAhbSram.

Table 1 · CoreAhbSram Release History

Version	Date	Changes
1.4	November 2008	Provided enhanced memory size options. Added user selection size ranging from 2048 to 32768 bytes, in steps of 2048 bytes.
1.3	August 2007	Added IGLOO, IGLOOe, and IGLOO PLUS support. Added ProASIC3L support. Provided additional memory size option of 8192 bytes.
1.2	–	Minor updates
1.1	–	Minor updates
1.0	–	First production release

Resolved Issues in the v1.4 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreAbhSram v1.4 release.

Table 2 · Resolved Issues in the v1.4 Release

SAR No	Description
78871	Additional memory size configuration options are now available. Memory size can now range from 2048 to 32768 bytes.
78888	The bus functional model (BFM) scriptlet packaged with this release has been enhanced to cover halfword (16 bit) writes to SRAM.

Known Issues and Workarounds

There are no known issues with CoreAbhSram.



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51300058-0/11.08

