RN0081

CoreAXItoAHBL v3.1 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Updated changes related to CoreAXItoAHBL v3.1.

1.2 Revision 4.0

Updated changes related to CoreAXItoAHBL v3.0.

1.3 Revision 3.0

Updated changes related to CoreAXItoAHBL v2.2.

1.4 Revision 2.0

Updated changes related to CoreAXItoAHBL v2.1.

1.5 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreAXItoAHBL v2.0.

Contents

2 CoreAXItoAHBL v3.1 Release Notes

2.1 Overview

These release notes accompany the production release of CoreAXItoAHBL v3.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Provides an interface (bridge) between the advanced extensible interface (AXI) domain and advanced high-performance lite bus (AHB-Lite) domain
- Makes alternate AXI write and AXI read transactions possible
- Supports AXI data bus width of 64-bits, with transfer size of 64/32-bit
- Maximum number of AXI beats or transfers of 16
- Supports unaligned AXI write / read transactions
- Permits the AXI and AHBL clocks to be derived from asynchronous sources
- Supports narrow transfers for the last transfer in AXI write transactions using write strobes
- Provides ERROR/OKAY response for every AXI master transaction
- Supports AHB data bus width of 32-bits
- Prevents sequential AHBL transfers from crossing 1 KB boundaries

2.3 Delivery Types

CoreAXItoAHBL is freely distributed with Microsemi Libero SoC. Complete HDL source code is provided for the core and testbenches.

2.4 Supported Families

- PolarFire
- IGLOO®2
- SmartFusion®2

2.5 Supported Tool Flows

CoreAXItoAHBL v3.1 requires Libero® System-on-Chip (SoC) software v11.0 or later.

2.6 Installation Instructions

The CoreAXItoAHBL CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreAXItoAHBL Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved History

Table 1 lists the release history for CoreAXItoAHBL.

Table 1 • **Release History**

Version	Date	Changes
3.1	November 2016	As listed in Table 2
3.0	December 2015	As listed in Table 3
2.2	September 2014	As listed in Table 4
2.1	June 2014	As listed in Table 5
2.0	February 2013	Initial Release.

2.10 Resolved Issues in the v3.1 Release

Table 2 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
82615	CoreAXItoAHBL need support for 32-bit AXI data transfer size.

2.11 Resolved Issues in the v3.0 Release

Table 3 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
69879	Complete re-design of the core. Unaligned address support added as part of the re-design.

2.12 Resolved Issues in the v2.2 Release

Table 4 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
58944	The core mishandles AXI bursts.

2.13 Resolved Issues in the v2.1 Release

Table 5 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
57249	RValid generation depending on RReady.

2.14 Discontinued Features and Devices

There are no discontinued features for this release of CoreAXItoAHBL v3.1.

2.15 Known Limitations and Workarounds

This release of CoreAXItoAHBL v3.1 does not support the following:

- A slave error will be returned to the AXI master, if a transfer of size other than 64-bit or 32-bit is attempted. The application can make use of the write strobes to write to locations, which are narrower than the transfer size.
- Narrow transfers using write strobes are not permitted for fixed address, AXI write transactions. For example, AWSIZE = 3’d3 (64-bit), WSTRB = 8’h7F and AWSIZE = 3’d2 (32-bit), WSTRB = 8’h07.
- Sparse assertion of the write strobes (holes in the write strobes) are not supported by the core. For example, WSTRB = 8’h5F (for 64-bit transfers), WSTRB = 8’h05 (for 32-bit transfers).

3 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

3.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world, **408.643.6913**

3.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

3.3 Technical Support

For Microsemi SoC Products Support, visit
http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support.

3.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/products/fpga-soc/fpga-and-soc.

3.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

3.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

3.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

3.5.3 Outside the U.S.

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