CoreAPB3 v4.1 Release Notes

This document accompanies the release of CoreAPB3 v4.1. It describes the features and enhancements of CoreAPB3 v4.1. This document contains information about the system requirements, supported families, implementations, and known issues and workarounds.

Features

- Supports up to 16 advanced peripheral bus (APB) slaves
- Supports master data bus width of 8, 16, or 32 bits
- Supports master address bus widths ranging from 12 bits to 32 bits
- Enables a master with an address bus width less than 32 bits to address a memory space of up to 4 Gbytes (2^{32} bytes) by indirect addressing
- Allows combination of several of the 16 slave slots to have access to all of these slots through a single slave interface

Interfaces

CoreAPB3 has a single APB mirrored master interface. This interface must be connected to an APB3 master. CoreAPB3 has 16 APB mirrored slave interfaces that can be connected to APB peripherals.

Microsemi® recommends using SmartDesign to connect and configure CoreAPB3 when creating a system design.

Delivery Types

CoreAPB3 is licensed in two ways: Obfuscated and register transfer level (RTL).

Obfuscated

Complete RTL code is provided for the core. This enables the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed within Libero® System-on-Chip (SoC). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core.

Supported Families

- SmartFusion®2
- SmartFusion
- Microsemi Fusion®
- IGLOO®
- IGLOO®e
- IGLOO®PLUS
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S
- IGLOO2
- RTG4™

Supported Tool Flows

Use Libero v8.6 or later with CoreAPB3 v4.1 release.

Installation Instructions

CoreAPB3 is available through the Libero SoC IP Catalog. Download it from a remote web-based repository to your local vault. Once installed in Libero SoC, you can instantiate, configure, connect, and generate the core using the SmartDesign tool.

New Features and Devices

- Support for IGLOO2 and RTG4 devices has been added.

Discontinued Features and Devices

No features or devices have been discontinued in this release.

Known Issues and Workarounds

There are no known issues in this release.

Release History

Table 1 provides the release history of CoreAPB3.

Table 1. Release History of CoreAPB3

Version	Date	Changes
4.1	December 2014	• Added RTG4 and IGLOO2 support
4.0	March 2013	• A greater range of memory space configurations are now supported. Slave slot size can range from 256 bytes to 256 Mbytes. • Combining of slave slots is now possible. This allows multiple regions of the memory map to be accessed through a single slave interface (S16). This feature may be useful when accessing MSS resources in a SmartFusion or SmartFusion2 SoC FPGA device. • More flexible indirect addressing support, and left shifting of the upper 4 address bits from the master is now available when the master address bus width is less than 32 bits.
3.0	February 2010	Added indirect addressing mode and capability to hide unused slots in SmartDesign canvas.
2.1	November 2006	Minor updates
2.0	June 2006	First production release

Resolved Issues in the v4.1 Release

There were no software action requests (SARs) resolved in this version. RTG4 support was added in this version.

Resolved Issues in the v4.0 Release

Table 2 lists the SARs that were resolved in the CoreAPB3 v4.0 release.

Table 2. Resolved SARs in CoreAPB3 v4.0 Release

SARs	Description
38846	Minor issue with docs packaging
40428	Indirect addressing feature through slave slot address is not consistent.
40429	Simulation loading error due to the improper part select statement in the RTL
41606	CoreAPB3: VHDL version has issues with indirect addressing
42977	Slot combining not working properly
42978	Can have ghost bits in slave address when bit shifting used
42979	BFM files missing from simulation file-sets for obfuscated license

Resolved Issues in the v3.0 Release

Table 3 lists the SARs that were resolved in the CoreAPB3 v3.0 release.

Table 3. Resolved SARs in CoreAPB3 v3.0 Release

SAR	Description
11962	CCZ Verification: Handbook not available.
14963	Validation should warn if all slots disabled.
23643	Add show/hide slave bus interfaces based on slot enable parameters.
23644	Add indirect addressing registers to allow full 32 bit PADDR access from one slot.
23690	XPATH equations needed to differentiate memory map slot addresses and ranges.
23737	PCLK and PRESETN inputs need to be added due addition of internal registers.

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