
CoreAI v3.0 Release Notes

This is the production release for CoreAI. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Key Features of CoreAI:

- ADC conversions controlled by MCU/MPU writes
- AMBA APB slave interface (8-, 16-, or 32-bit widths supported)
- 7 maskable interrupt sources
- Analog configuration MUX can be configured from the Catalog in the Libero IDE Project Manager
- Ability to disable/enable AB macro during power-up

Interfaces

CoreAI is available with an advanced microcontroller bus architecture (AMBA) APB slave interface.

Delivery Types

CoreAI is licensed in the following two ways.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole or SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero[®] Integrated Design Environment (IDE). The RTL code for the core is obfuscated and some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion

Supported Tool Flows

This version requires the following base versions of tools:

- Libero IDE v8.5 or higher
- CoreConsole v1.4 (optional)

Install Instructions

The CoreAI CCZ file must be installed using either the CoreConsole IDP or Libero IDE.

CoreConsole Instructions

Close all CoreConsole projects and use Actions > Add to database in CoreConsole to locate and install a local CCZ file, or use the automatic web update feature in CoreConsole. Once the CCZ file is installed in CoreConsole, the core can be instantiated, configured, and exported to the Libero IDE environment.

For the RTL release version of the core, the FlexLM license must be installed and Libero IDE restarted before the core can be configured and generated within CoreConsole. Refer to the Libero IDE online help for instructions about core installation and licensing.

Libero IDE/SmartDesign Instructions

Within Libero IDE, click the Add Core button in the Catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

For the RTL release version of the core, the FlexLM license must be installed and Libero IDE restarted before the core can be configured and generated within SmartDesign. Refer to the Libero IDE online help for instructions about core installation and licensing.

Documentation

This release contains a copy of the CoreAI Handbook, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions. If using CoreConsole, the documentation can be viewed by right-clicking the Core Selection window in CoreConsole after the core has been installed. If using SmartDesign, refer to the Libero IDE online help for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website, <http://www.actel.com>.

Supported Test Environments

This version supports the following environments:

- Verilog user testbench
- VHDL user testbench

Discontinued Features and Devices

The optional 256-element FIFO that was available in a previous release of CoreAI has been removed. For details on how to implement similar functionality with this release of CoreAI, refer to the latest CoreAI handbook.

New Features and Devices

The following features have been added:

- Support for optional hardware-driven inputs
- Support for AFS090 and AFS250 Fusion devices
- Ability to remove interrupt logic when not used
- Ability to set ACM clock frequency given PCLK frequency
- Support for shifting ADC result bits
- Support for disabling/enabling AB macro during power-up

Release History

Table 1 details the release history of this core.

Table 1 · CoreAI Release History

Version	Date	Changes
3.0	January 2009	Numerous fixes and packaging updates, including SmartDesign support. Refer to Table 2 for details.
2.1	June 2006	Simulation issue fixed related to using read FIFO with obfuscated license.
2.0	April 2006	First production release.

Resolved Issues in the v3.0 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the v3.0 release of CoreAI.

Table 2 · Resolved Issues in the CoreAI v3.0 Release

SAR	Description
11393	When disabling CFG_ACx, CFG_ATx parameters, CMSTBx, TMSTBx need grounds.
11397	Addition of BUSY output to indicate when CoreAI is busy.
11533	Shift internal address map to accommodate 32,16,8-bit addresses.
11531	Add more hardware-driven inputs and change name of DDGDON to HD_GDON.
11532	Bring out some internal connections to/from AB macro.
11534	Remove read FIFO and all associated logic.
11535	Add parameter to shift RESULT[11:0] bits in ADC status register.
11398	Add parameter to remove interrupt logic when not used.
12090	CoreAI packaging does not allow external VAREF
11501	Add RTC configuration options in IP configuration dialog
13673	Add optional logic gate AB SYSCLK: allow VAREF cap to rise to 2.56V per Fusion datasheet
13674	Add 1/2 cycle PCLK delay to ADCRESET and ADCSTART signals connected to AB macro

Resolved Issues in the v2.1 Release

The v2.1 release fixes a simulation issue that manifested itself when the read FIFO was used with an obfuscated license.

Resolved Issues in the v2.0 Release

This was the first core production release; hence there are no resolved issues from a previous release.

Known Issues in the v3.0 Release

AB Simulation Model Warnings and Errors

You may see simulation warnings and errors in the user testbench related to the ADC clock frequency and the AC, AT, and AV prescaler opamps. These warning and error messages come from the AB (analog block) simulation model and can be safely ignored.

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