CoreAHBtoAPB3 v2.0

Handbook

Actel
POWER MATTERS

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Trademarks

Table of Contents

Introduction

CoreAHBtoAPB3 is an AHB slave and AMBA 3 APB master that provides an interface (bridge) between the high-speed AHB domain and the low-power APB domain. The CoreAHBtoAPB3 interfaces with CoreAHB/CoreAHBLite through the AHB interface, or CoreAPB3 through the APB interface.

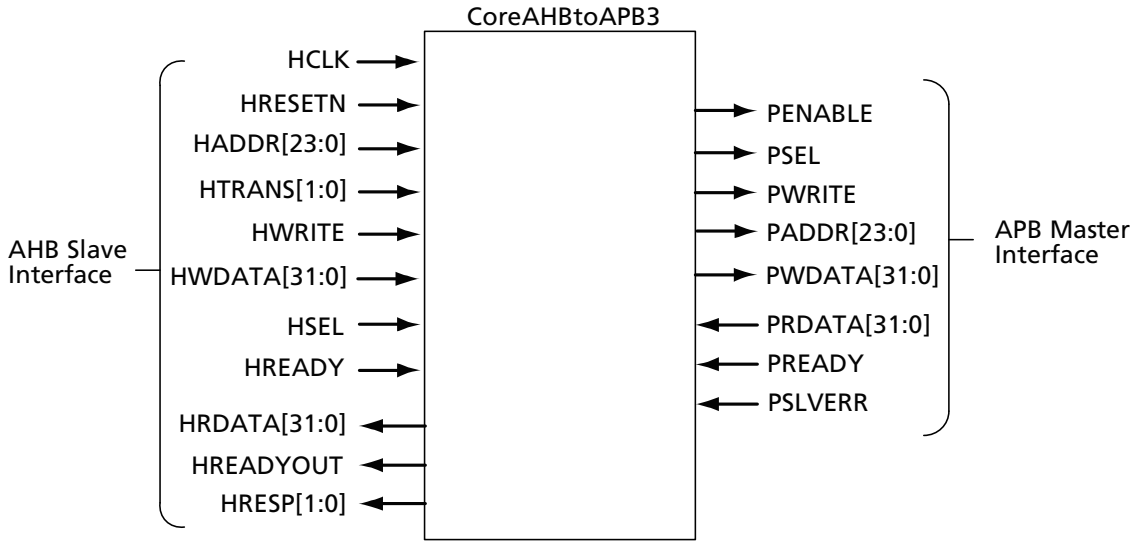

Figure 1 CoreAHBtoAPB3 I/O Signal Diagram

Key Features

- Bridges between Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus (APB).
- Automatic connection to CoreAHB/CoreAHBLite and CoreAPB3 in SmartDesign
- AMBA 3 APB compliant

Core Version

This handbook supports CoreAHBtoAPB3 v2.0.

Supported Interfaces

CoreAHBtoAPB3 supports an AHB or AHB-Lite slave interface connected to an AHB or AHB-Lite mirrored slave interface (for example, CoreAHB or CoreAHBLite) as well as an AMBA 3 APB master interface that connects to an AMBA3 APB mirrored master interface (for example, CoreAPB3).

Utilization and Performance

CoreAHBtoAPB3 has been implemented in several of Actel's device families using standard speed grades. A summary of various implementation data is listed in Table 1.

Table 1 CoreAHBtoAPB3 Device Utilization and Performance

Family	Tiles			Utilization		Performance MHz
	Sequential	Combinatorial	Total	Device	Total %	
Fusion	126	75	201	M1AFS1500	1%	128
IGLOO®/e, IGLOO PLUS	126	80	206	M1AGL1000V2	1%	75
ProASIC®3/E/L	126	72	198	M1A3P600	1%	134
ProASIC PLUS®	128	192	320	APA600	1%	80
Axcelerator®	127	72	199	AX500	2%	145
RTAX-S	127	72	199	RTAX1000S	1%	97

Note: Data in this table were achieved with typical synthesis and layout settings.

Design Description

I/O Signals

The port signals for the CoreAHBtoAPB3 macro are illustrated in Figure 1 on page 5 and defined in Table 2.

Table 2 CoreAHBtoAPB3 I/O Signal Descriptions

Port Name	Type	Description
AHB Interface		
HCLK	In	AHB clock. All AHB signals are synchronous to the rising edge of this clock signal.
HRESETN	In	AHB asynchronous reset. This is an active low signal.
HADDR[23:0]	In	AHB address bus
HTRANS[1:0]	In	AHB transfer type from the master. Indicates the type of current transfer: 00 – Idle 01 – Busy 10 – Non-sequential 11 – Sequential
HWRITE	In	AHB write/read. If High, a write takes place; if Low, a read takes place.
HWDATA[31:0]	In	AHB write data
HSEL	In	AHB slave select. This signal selects slave for reads or writes.
HREADY	In	AHB ready input signal from the master
HRDATA[31:0]	Out	AHB read data
HREADYOUT	Out	AHB ready signal to the master. When High, the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven Low to extend a transfer.
HRESP[1:0]	Out	AHB transfer response to the master: 00 – Okay 01 – Error 10 – Retry 11 – Split
APB Interface		
PADDR[23:0]	Out	APB address bus
PSEL	Out	APB slave select; select signal for register for reads or writes.
PENABLE	Out	APB strobe. This signal indicates the second cycle of an APB transfer.

Port Name	Type	Description
PWRITE	Out	APB write/read. If High, a write occurs when an APB transfer takes place. If Low, a read takes place.
PWDATA[31:0]	Out	APB write data
PRDATA[31:0]	In	APB read data
PREADY	In	APB ready. Used to insert wait states.
PSLVERR	In	APB Error. If High, indicates an error condition on an APB transfer. If a peripheral does not include a PSLVERR pin, this pin must be tied Low.

Note: All signals are active High (logic 1) unless otherwise noted.

Design Details

CoreAHBtoAPB3 (AMBA bridge) is an AHB slave that links the AHB bus to the APB bus and acts as the master on the APB bus. Read and write transfers on the AHB bus are converted to corresponding transfers on the APB bus. High bandwidth peripherals, such as memory controllers, are typically connected to the AHB, whereas the APB bus is used for less demanding peripherals, such as watchdogs. Unlike the AHB bus, transfers on the APB bus are not pipelined.

AHB Interface Timing

The AHB interface is compliant with the AMBA specification.

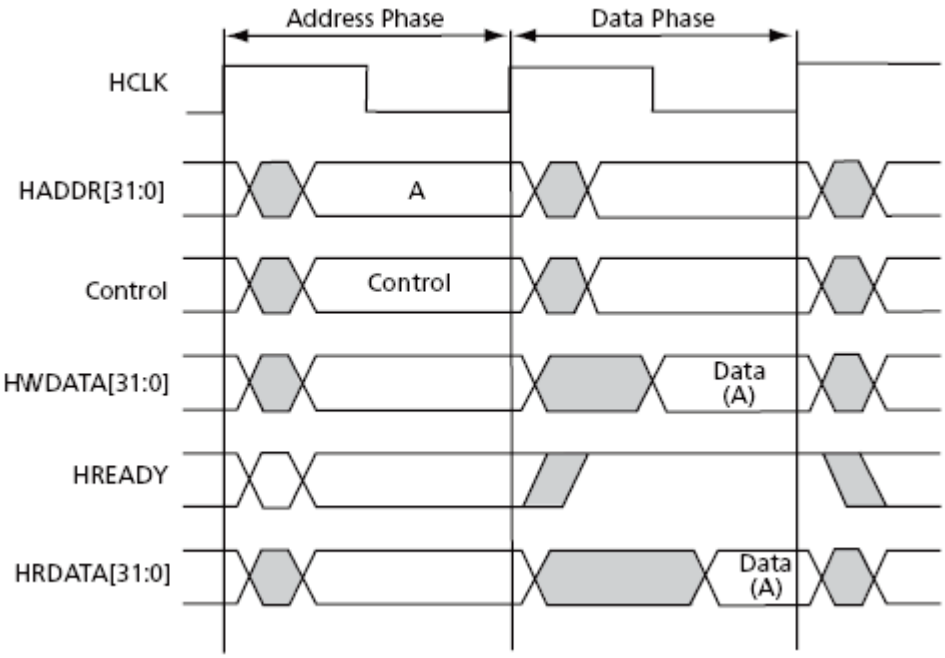

Figure 2 Simple Transfer

More detailed descriptions and timing waveforms can be found in the AMBA specification: http://www.amba.com/products/solutions/AMBA_Spec.html.

APB Interface Timing

The APB interface is compliant with the AMBA specification. Figure 3 and Figure 4 depict typical write cycle and read cycle timing relationships relative to the system clock, PCLK.

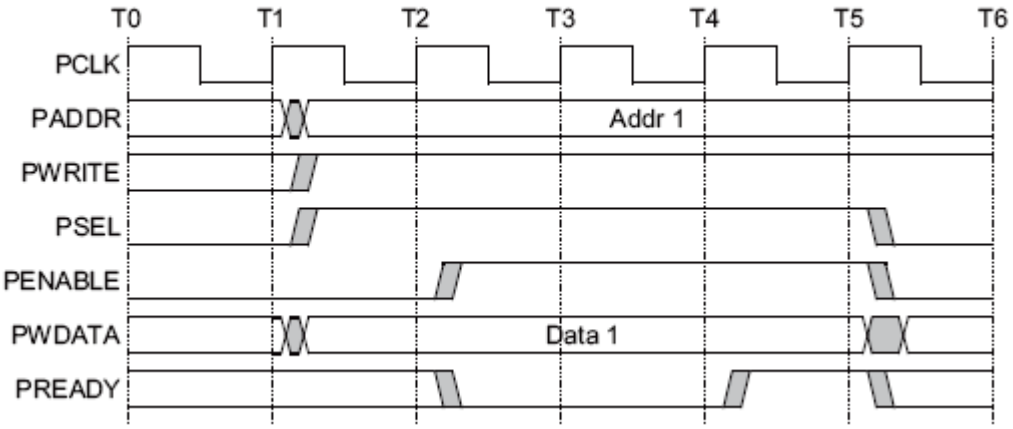

Figure 3 APB Write Transfer with Wait States

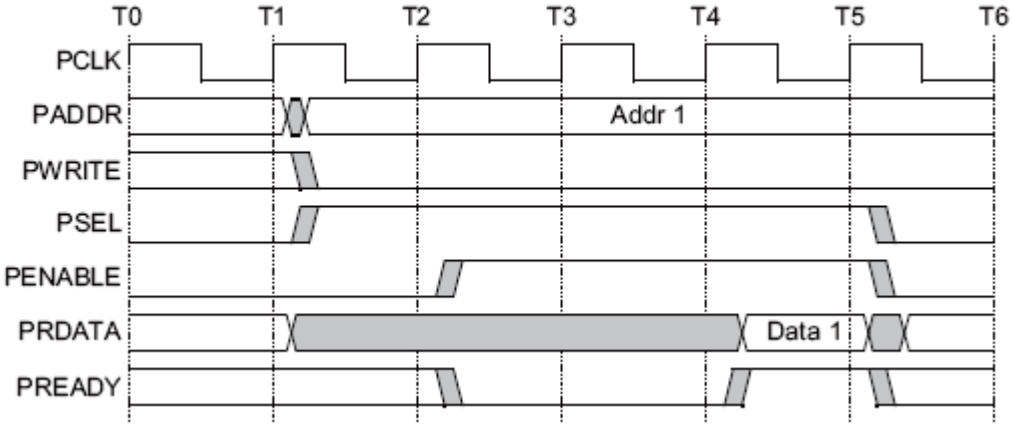

Figure 4 APB Read Transfer with Wait States

AHB to APB Bridge Interface Timing

Figure 5 depicts write cycle and read cycle timing relationships relative to the system clock, HCLK. The data “12345678” was written and read back by the AHB master from the APB slave through the AHB to APB bridge. The read and write cycles are shown betweeen the two cursors.

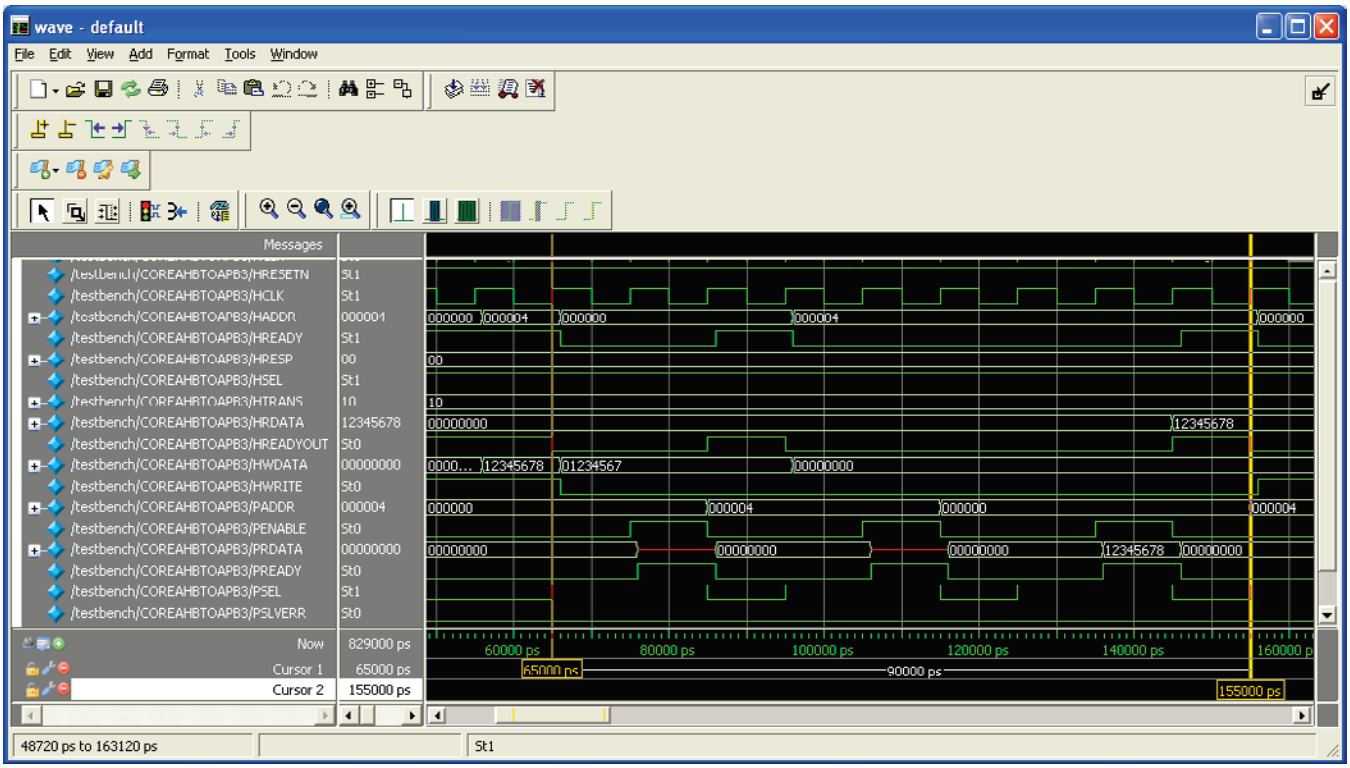

Figure 5 AHB to APB Write and Read Data Cycles

Tool Flows

Licensing

CoreAHBtoAPB3 is licensed in two ways. Depending on your license tool flow, functionality may be limited.

Obfuscated

Complete RTL code is provided for the core, allowing the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed within Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated[1] and some of the testbench source files are not provided; they are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

SmartDesign

CoreAHBtoAPB3 (Figure 6 on page 14) is preinstalled in the SmartDesign IP Deployment design environment. The core can be configured using the configuration GUI within SmartDesign (Figure 7 on page 14). For more information on using SmartDesign to instantiate and generate cores, refer to the Using DirectCore in Libero® IDE User's Guide.

1 *Obfuscated means the RTL source files have had formatting and comments removed, and all instance and net names have been replaced with random character sequences.*

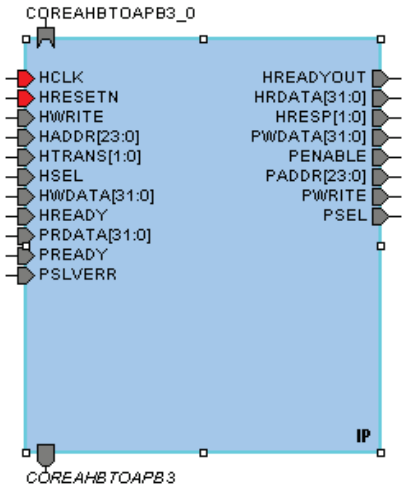

Figure 6 CoreAHBtoAPB3 Full I/O View

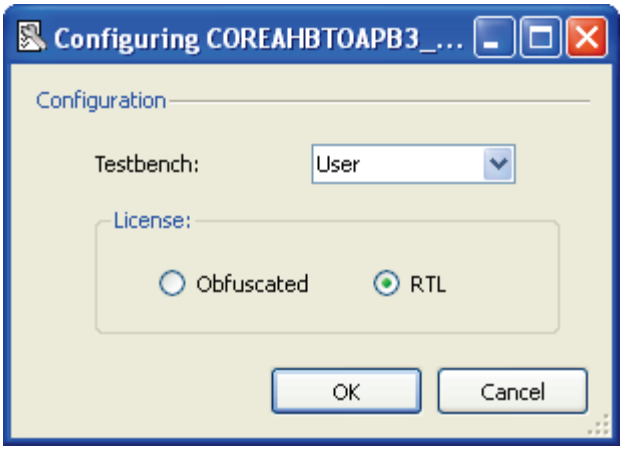

Figure 7 CoreAHBtoAPB3 SmartDesign Configuration

Simulation Flows

The User Testbench for CoreAHBtoAPB3 is included in all releases.

To run simulations, select the User Testbench flow within SmartDesign and click **Save & Generate** on the Generate pane. The User Testbench is selected through the Core Testbench Configuration GUI.

When SmartDesign generates the Libero IDE project, it installs the user testbench files.

To run the user testbench, set the design root to the CoreAHBtoAPB3 instantiation in the Libero IDE design hierarchy pane and click the Simulation icon in the Libero IDE Design Flow window. This invokes ModelSim® and automatically runs the simulation.

User Testbench

The simulation environment is shown in Figure 8 and includes instantiation of the CoreAHBtoAPB3 macro, AHB-Lite master BFM, and APB slave bus functional model (BFM). Included with the release of CoreAHBtoAPB3 is a user testbench that gives an example of how to use the core with the master. The user testbench, as shown in Figure 8, instantiates a behavioral Actel DirectCore AMBA BFM module to emulate an AHB-Lite master on the AHB port and an APB BFM on the APB port of CoreAHBtoAPB3.

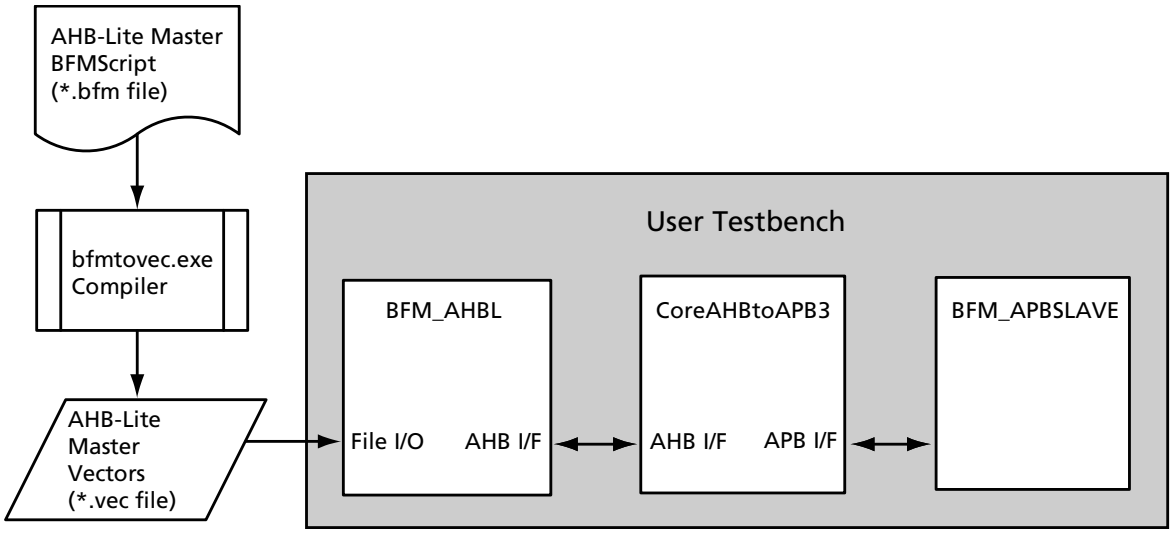

Figure 8 CoreAHBtoAPB3 User Testbench

A BFM ASCII script source file (*.bfm file), with comments, is included in the directory. You can find the script source file in *YourLiberoProjectDirectory*/*COREAHBTOAPB3*/*mti*/*scripts*, where "YourLiberoProjectDir" represents the path to your Libero IDE project that uses CoreAHBtoAPB3.

The BFM source file controls the AHB-Lite master and is named master.bfm. The BFM source file is automatically recompiled each time the simulation is invoked from Libero IDE by the bfmtovec.exe executable, if running on a Windows® platform, or by the bfmtovec.lin executable, if running on a Linux platform. The output *.vec vector file, created by the bfmtovec.exe executable, is read in by the BFM module for simulation in ModelSim.®

You can alter the BFM script, if desired. Refer to the *Actel DirectCore AMBA BFM User's Guide* for more information.

The source code for the user testbench and BFM script is available with the CoreAHBtoAPB3 Obfuscated and RTL releases. A compiled ModelSim simulation library containing the BFM modules is available with the CoreAHBtoAPB3 Obfuscated release. An obfuscated RTL version of the BFM modules is available with the CoreAHBtoAPB3 RTL release.

Synthesis in Libero IDE

Having set the design route appropriately, click the **Synthesis** icon in Libero IDE. The Synthesis window appears, displaying the Synplicity® project. Set Synplicity to use the Verilog 2001 standard if Verilog is being used. To run Synthesis, select the **Run** icon.

Place-and-Route in Libero IDE

Having set the design route appropriately and run Synthesis, click the **Layout** icon in the Libero IDE to invoke Designer. CoreAHBtoAPB3 requires no special place-and-route settings.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure

to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

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