CoreAHBLtoAXI v2.1 Release Notes

This release note accompanies the production release for CoreAHBLtoAXI v2.1 IP core. This document provides details about the features, supported families, system requirements, implementations, and known limitations and workarounds.

Features

CoreAHBLtoAXI is a highly configurable core and has the following features:

- An interface (bridge) between the advanced high-performance bus (AHB) domain and advanced extensible interface (AXI) domain.
- SINGLE/INCR/WRAP type write transactions.
- SINGLE/INCR/WRAP type read transactions.
- WRAP type transactions for word size accesses only. WRAP for half word and byte size accesses are not supported in this release.
- Undefined length Increment bursts on the AHBL are converted only into single burst transfer. INCR transactions of 64-bit size and burst length UPTO 16 are not supported in this release.

Delivery Types

CoreAHBLtoAXI is licensed as register transfer level (RTL).

RTL

Complete RTL source code is provided for the core and test benches.

Supported Families

- SmartFusion®2
- IGLOO®2

Supported Tool Flows

Libero® System-on-Chip (SoC) software v11.0 or later supports the CoreAHBLtoAXI v2.1 release.

Installation Instructions

For the RTL version of the core, the FlexLM license must be installed before the core can be exported. Consult the Libero SoC online help for the instructions on core installation and licensing.

Documentation

This release contains a copy of the *CoreAHBLtoAXI handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi web site at: http://www.microsemi.com/soc.

Supported Test Environments

- Verilog User Testbench
- VHDL User Testbench

Discontinued Features and Devices

There are no discontinued features for release of v2.1.

Known Limitations

This release of CoreAHBLtoAXI v2.1 does not support the following:

- wrap transfer size for half-word and byte
- AHB data width of 64 bits
- UNDEF_BURST = 1 is not supported

Release History

There are resolved issues in the CoreAHBLtoAXI v2.1 release.

Table 1 Release History

Version	Date	Changes
2.1	June 2014	As listed in Table 2.
2.0	February 2013	Initial release.

Resolved Issues in the v2.1 Release

Table 2 lists the software action requests (SARs) that were resolved in the CoreAHBLtoAXI v2.1 release.

Table 2 Resolved SARs in CoreAXItoAHBL v2.1 Release

SAR	Description
57250	Issue with generation of WLAST signal.

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