HB0144
Handbook
CoreAHBLite v5.3

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Power Matters.

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 10.0

Updated changes related to CoreAHBLite v5.3. Added information about PolarFire support.

1.2 Revision 9.0

Updated changes related to CoreAHBLite v5.2. Added information about IGLOO2 and RTG4 support.

1.3 Revision 8.0

Updated changes related to CoreAHBLite v5.0. Added two more master interfaces. CoreAHBLite can now support a total of four masters.

1.4 Revision 7.0

Updated changes related to CoreAHBLite v4.0.

A greater range of memory space configurations is now supported. Slave slot size can range from 256 bytes to 256 Mbytes.

Mode with 16 x 64 Kbyte slots along with one huge (2 GByte) slot is still supported, but initialization interfaces located from 0x00040000 - 0x0004FFFF are no longer supported in this mode.

Combining of slave slots is now possible. This allows multiple regions of the memory map to be accessed through a single slave interface (S16). This feature may be useful while accessing MSS resources in the SmartFusion or SmartFusion2 device.

1.5 Revision 6.0

Updated changes related to CoreAHBLite v3.1. Added capability for memory maps to be altered in SmartDesign to reflect the value of the MODE_CFG parameter.

1.6 Revision 5.0

Updated changes related to CoreAHBLite v3.0. Added another memory configuration mode. Added huge slot capability and Init/Config client support.

1.7 Revision 4.0

Updated changes related to CoreAHBLite v2.0. Added multi-master capability and additional ports to satisfy multi-master capability.

1.8 Revision 3.0

Updated changes related to CoreAHBLite v1.3. Minor updates.

1.9 Revision 2.0

Updated changes related to CoreAHBLite v1.2. Minor updates.

1.10 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreAHBLite v1.1.

2 Preface

2.1 About this Document

This handbook provides details about the CoreAHBLite DirectCore module, and how to use it.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

2.3 References

2.3.1 Third Party Publications

- ARM AMBA 3 AHB-Lite Protocol Specification v1.0

3 Overview

CoreAHBLite implements an advanced microcontroller bus architecture (AMBA) AHB-Lite bus interconnect fabric. CoreAHBLite provides four master interfaces and can accommodate up to 16 slave interfaces. Each slave interface can be enabled or disabled for each master using the configuration graphical user interface (GUI) of the core. Slave interfaces that are not enabled do not appear for connection on the CoreAHBLite symbol and are optimized away during the synthesis. Similarly, if no slave interfaces are selected for a given master, then that master interface is disabled and optimized away during the synthesis.

CoreAHBLite supports the following memory space scenarios:

- 16 64 KB slave slots, some reserved space, and 1 huge 2 GB slave slot
- 4 GB address space apportioned into 16 slave slots, each of size 256 MB
- 256 MB address space apportioned into 16 slave slots, each of size 16 MB
- 16 MB address space apportioned into 16 slave slots, each of size 1 MB
- 1 MB address space apportioned into 16 slave slots, each of size 64 KB
- 64 KB address space apportioned into 16 slave slots, each of size 4 KB
- 4 KB address space apportioned into 16 slave slots, each of size 256 KB

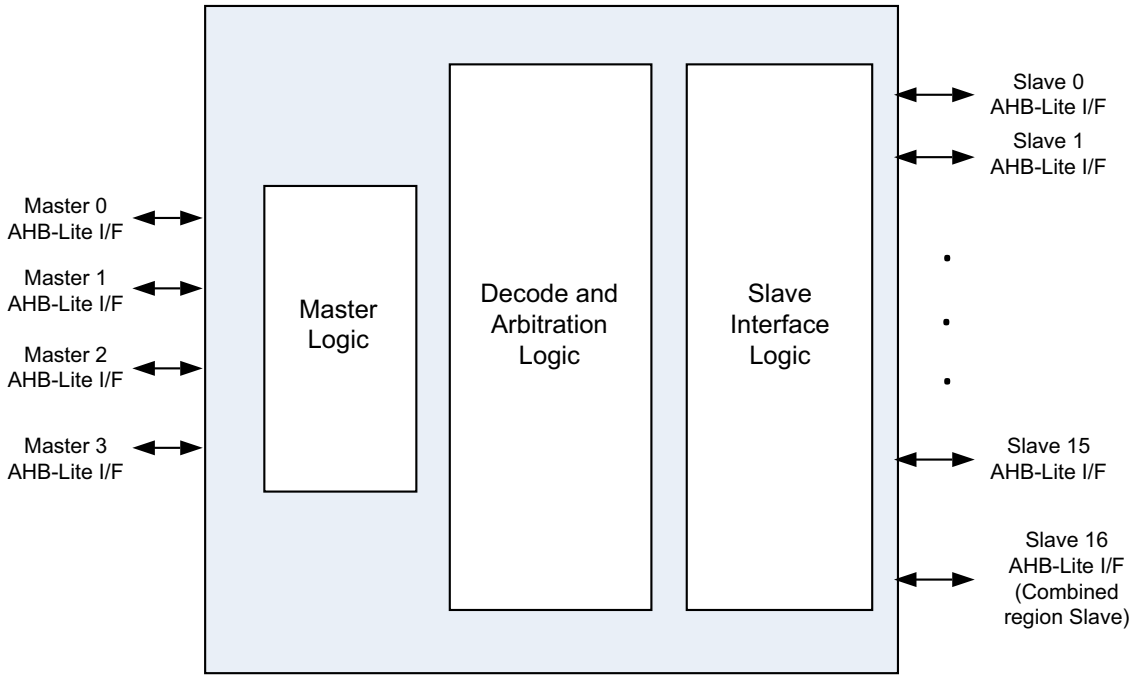
For all cases except the first option listed above, it is possible to allocate one or more slave slots to a combined region slave interface. When some slave slots have been assigned to the combined region, an additional slave interface becomes available for connection. This feature allows a number of (possibly noncontiguous) regions of the memory space to be associated with a single slave interface. This may be useful, in a SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device, where a master located in the FPGA fabric wants to access a number of resources in the microcontroller subsystem (MSS) through a single slave interface.

The first memory space configuration listed above is useful in a SmartFusion SoC FPGA device. The 16 64 KB slave slots occupy a total address space of 16*64*1024 = 2^{20} bytes and this suits the 20-bit address bus provided in the interface from the SmartFusion MSS to the FPGA fabric. The huge (2 GB) slave slot is useful in the opposite direction, that is, when a master based on the FPGA fabric needs to access resources in the SmartFusion MSS device.

CoreAHBLite provides a remapping facility for its master 0 connection. When remapping is enabled (by holding the REMAP_M0 input of the core High), slave slots 0 and 1 are swapped over from the viewpoint of master 0. This feature is typically used to swap memory resources between slots 0 and 1 when a processor is connected to the master 0 interface.

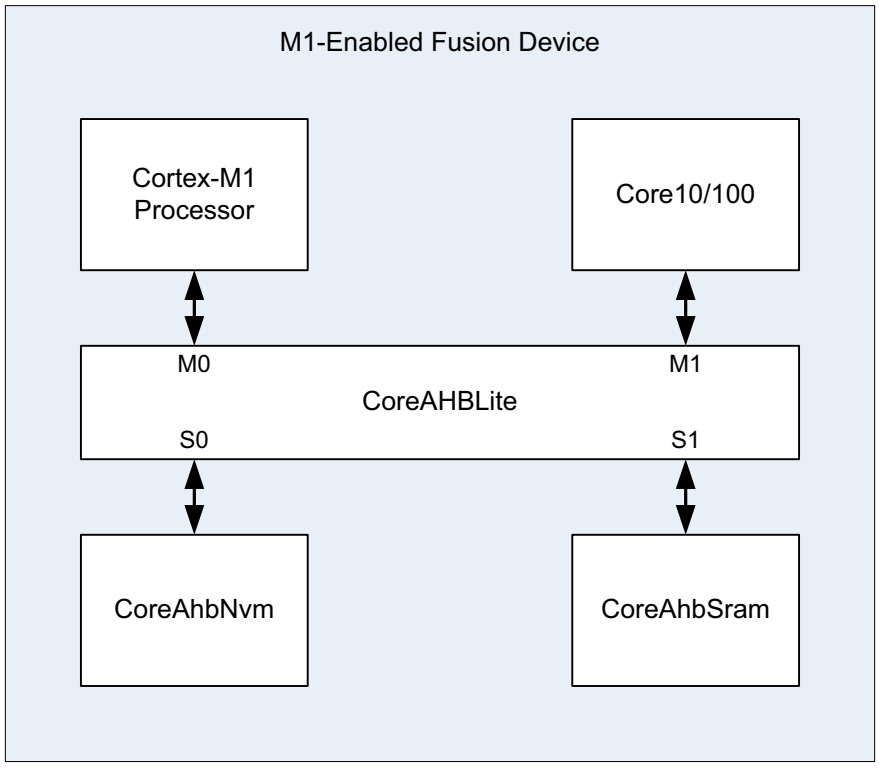
The following figure shows the block diagram of CoreAHBLite.

Figure 1 • **CoreAHBLite Block Diagram**



The following figure shows a typical application using CoreAHBLite.

Figure 2 • **CoreAHBLite Typical Application**



3.1 Key Features

Following are the key features of CoreAHBLite:

- Supports four masters
- Supports up to 16 slaves (up to 17 in one mode, if the huge slave is in use)
- Address space per slave varies from 256 bytes to 256 MB (huge slave occupies 2 GB.)
- Supports allocation of slave slots to a combined region slave interface in most modes
- Enable access to any slave slot on a per master basis
- Equal priority for all masters (round-robin arbitration scheme)
- Supports remapping feature for master 0 interface

3.2 Supported Families

The following families are supported in this version:

- PolarFire™
- RTG4™
- SmartFusion®2
- IGLOO®2
- SmartFusion®
- IGLOO®
- IGLOO®e
- IGLOO® PLUS
- Fusion®
- ProASIC®3
- ProASIC®3E
- ProASIC®3L
- Axcelerator®
- RTAX-S

3.3 Core Version

This handbook supports CoreAHBLite v5.3.

3.4 Supported Interfaces

CoreAHBLite supports four AHB-Lite master interfaces and up to 16 AHB-Lite slave interfaces (up to 17 slave interfaces are supported in one mode when the huge slave is in use).

Microsemi recommends using the SmartDesign tool to connect and configure CoreAHBLite while creating a system design.

3.5 Utilization and Performance

Utilization and performance data is provided in the following tables. The data is indicative only. CoreAHBLite is a bus component that interconnects between master and slave devices. The overall device utilization and performance of a system is very much system dependent.

Table 1 • **CoreAHBLite Device Utilization and Performance (Minimum Configuration, 1 Master and 1 Slave)**

	FPGA Resources			Utilization		
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**Performance (MHz)**
SmartFusion2	62	171	242	M2S150T	0.16	129.9
IGLOO2	62	171	242	M2GL150T	0.16	129.1
RTG4	67	185	246	RT4G150	0.16	115.4
IGLOO/e	74	265	328	M1AGLE3000V2	0.45	28.7
ProASIC3/E	72	262	331	M1A3P1000	1.36	65.8

Table 1 • **CoreAHBLite Device Utilization and Performance (Minimum Configuration, 1 Master and 1 Slave) *(continued)***

	FPGA Resources			Utilization		Performance
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**(MHz)**
ProASIC3L	74	264	338	M1A3P1000L	1.38	85.7
Fusion	72	262	331	M1AFS1500	0.87	65.8
ProASIC^{PLUS}	76	373	449	APA1000	1	47
Axcelerator	80	238	318	AX1000	2	141.8
RTAX-S	79	240	319	RTAX1000S	2	161.2
PolarFire	62	175	237	MPF300T	0.08	169.6

Table 2 • **CoreAHBLite Device Utilization and Performance (Typical Configuration, 1 Master and 4 Slaves)**

	FPGA Resources			Utilization		Performance
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**(MHz)**
SmartFusion2	82	545	724	M2S150T	0.43	111.8
IGLOO2	82	545	724	M2GL150T	0.43	111.8
RTG4	106	634	680	RT4G150	0.49	102.4
IGLOO/e	125	791	916	M1AGLE3000V2	1.22	23.7
ProASIC3/E	125	736	861	M1A3P1000	3.50	64.2
ProASIC3L	125	792	917	M1A3P1000L	3.73	67.0
Fusion	128	860	988	M1AFS1500	2.57	64.0
ProASIC^{PLUS}	127	899	1026	APA1000	2	40.9
Axcelerator	150	652	802	AX1000	5	119.6
RTAX-S	150	651	801	RTAX1000S	5	136.9
PolarFire	79	567	646	MPF300T	0.22	147.8

Table 3 • **CoreAHBLite Device Utilization and Performance (two masters and 16 slaves)**

	FPGA Resources			Utilization		Performance
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**(MHz)**
SmartFusion2	215	2005	2220	M2S150T	1.52	105.1
IGLOO2	261	2053	2314	M2GL150T	1.58	95.5
RTG4	288	2164	2452	RT4G150	1.62	99.8
IGLOO/e	381	2751	3132	M1AGLE3000V2	4.16	24.5
ProASIC3/E	381	2809	3190	M1A3P1000	12.98	50.0
ProASIC3L	386	2929	3315	M1A3P1000L	13.49	56.3
Fusion	387	2954	3341	M1AFS1500	8.7	51.6
ProASIC^{PLUS}	394	3293	3687	APA1000	6	37
Axcelerator	453	2399	2852	AX1000	16	83.8
RTAX-S	370	2320	2690	RTAX1000S	15	87.9
PolarFire	216	2191	2407	MPF300T	0.80	135.5

Table 4 • **CoreAHBLite Device Utilization and Performance (three masters and 16 slaves)**

	FPGA Resources			Utilization		Performance
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**(MHz)**
SmartFusion2	345	2148	2493	M2S150T	1.71	102.3
IGLOO2	284	2094	2378	M2GL150T	1.62	100
RTG4	341	2206	2547	RT4G150	1.67	82.8
IGLOO/e	434	3199	3633	M1AGLE3000V2	4.83	22.5
ProASIC3/E	427	2984	3411	M1A3P1000	13.88	52.1
ProASIC3L	421	2795	3216	M1A3P1000L	13.09	61.8
Fusion	430	2907	3337	M1AFS1500	8.69	52
ProASIC^{PLUS}	432	3262	3694	APA1000	6	38.4
Axcelerator	424	2394	2818	AX1000	16	85.2
RTAX-S	443	2474	2917	RTAX1000S	17	100.9
PolarFire	306	2057	2363	MPF300T	0.79	139.9

Table 5 • **CoreAHBLite Device Utilization and Performance (four masters and 16 slaves)**

	FPGA Resources			Utilization		Performance
Family	**Sequential**	**Combinatorial**	**Total**	**Device**	**%**	**(MHz)**
SmartFusion2	342	2143	2485	M2S150T	1.70	105.3
IGLOO2	342	2252	2594	M2GL150T	1.77	106.7
RTG4	374	2275	2649	RT4G150	1.75	102.9
IGLOO/e	498	3167	3665	M1AGLE3000V2	4.87	25.4
ProASIC3/E	498	3192	3690	M1A3P1000	15.01	63.1
ProASIC3L	500	3214	3714	M1A3P1000L	15.11	56.0
Fusion	501	3164	3665	M1AFS1500	9.54	53.4
ProASICPLUS	501	3365	3866	APA1000	7	39
Axcelerator	502	2624	3126	AX1000	18	78.3
RTAX-S	518	2765	3283	RTAX1000S	19	97.3
PolarFire	331	2153	2484	MPF300T	0.83	143.0

4 Interface Description

4.1 Configuration Parameters

The register transfer level (RTL) code for CoreAHBLite has parameters for configuring the core. While working with the core in the SmartDesign tool, a configuration GUI is used to set the values of these parameters. CoreAHBLite parameters are listed in the following table.

Table 6 • **CoreAHBLite Configuration Parameters**

Parameter Name	Valid Range	Default	Description
MEMSPACE	0 to 6	0	0: 16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000 1: 4 GB addressable space apportioned into 16 slave slots, each of size 256 MB 2: 256 MB addressable space apportioned into 16 slave slots, each of size 16 MB 3: 16 MB addressable space apportioned into 16 slave slots, each of size 1 MB 4: 1 MB addressable space apportioned into 16 slave slots, each of size 64 KB 5: 64 KB addressable space apportioned into 16 slave slots, each of size 4 KB 6: 4 KB addressable space apportioned into 16 slave slots, each of size 256 B
HADDR_SHG_CFG	0 or 1	1	This parameter is only relevant when MEMSPACE = 0. 0: HADDR_S16[31] tied low, huge slave address range is 0x00000000 - 0x7FFFFFFF from slave perspective. 1: HADDR_S16[31] tied high, huge slave address range is 0x80000000 - 0xFFFFFFFF from slave perspective.
M0_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 0 1: Enables slave 0 for master 0
M0_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 0 1: Enables slave 1 for master 0
…	…	…	…
M0_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 0 1: Enables slave 15 for master 0
M0_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 0 1: Enables slave 16 for master 0 (Slave 16 is the combined region slave or huge slave.)
M1_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 1 1: Enables slave 0 for master 1
M1_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 1 1: Enables slave 1 for master 1
…	…	…	…
M1_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 1 1: Enables slave 15 for master 1
M1_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 1 1: Enables slave 16 for master 1 (Slave 16 is the combined region slave or huge slave.)

Table 6 • **CoreAHBLite Configuration Parameters *(continued)***

Parameter Name	Valid Range	Default	Description
M2_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 2 1: Enables slave 0 for master 2
M2_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 2 1: Enables slave 1 for master 2
…	…	…	…
M2_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 2 1: Enables slave 15 for master 2
M2_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 2 1: Enables slave 16 for master 2 (Slave 16 is the combined region slave or huge slave.)
M3_AHBSLOT0ENABLE	0 or 1	0	0: Disables slave 0 for master 3 1: Enables slave 0 for master 3
M3_AHBSLOT1ENABLE	0 or 1	0	0: Disables slave 1 for master 3 1: Enables slave 1 for master 3
…	…	…	…
M3_AHBSLOT15ENABLE	0 or 1	0	0: Disables slave 15 for master 3 1: Enables slave 15 for master 3
M3_AHBSLOT16ENABLE	0 or 1	0	0: Disables slave 16 for master 3 1: Enables slave 16 for master 3 (Slave 16 is the combined region slave or huge slave.)
SC_0	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 0 to the combined region. 0: Slave slot 0 is not assigned to the combined region. Slave interface 0 is available for connection if enabled. 1: Slave slot 0 is assigned to the combined region. Slave interface 16 is available for connection if enabled, but slave interface 0 is not available for connection.
SC_1	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 1 to the combined region. 0: Slave slot 1 is not assigned to the combined region. Slave interface 1 is available for connection if enabled. 1: Slave slot 1 is assigned to the combined region. Slave interface 16 is available for connection if enabled, but slave interface 1 is not available for connection.
…	…	…	…
SC_15	0 or 1	0	This parameter is only relevant when MEMSPACE > 0. This parameter can be used to assign slave slot 15 to the combined region. 0: Slave slot 15 is not assigned to the combined region. Slave interface 15 is available for connection if enabled. 1: Slave slot 15 is assigned to the combined region. Slave interface 16 is available for connection if enabled, but slave interface 15 is not available for connection.

4.2 Ports

The following table lists the ports present on CoreAHBLite.

Table 7 • **CoreAHBLite Ports [1]**

Port Name	Type	Description
HRESETN	Input	AHB-Lite reset active low asynchronous reset.
HCLK	Input	AHB-Lite clock signal. All AHB-Lite interface signals are synchronous to the rising edge of this clock.
HADDR_M0[31:0]	Input	AHB-Lite address bus for master 0.
HMASTLOCK_M0	Input	AHB-Lite locked sequence indication for master 0.
HSIZE_M0[2:0]	Input	AHB-Lite transfer size for master 0. Indicates the size of the transfer. Only byte, half-word, and word transactions are supported.
HTRANS_M0[1:0]	Input	AHB-Lite transfer type for master 0. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M0	Input	AHB-Lite write indication for master 0. High for a write, Low for a read.
HWDATA_M0[31:0]	Input	AHB-Lite write data for master 0.
HBURST_M0[2:0]	Input	AHB-Lite burst type for master 0. Indicates if the transfer forms part of a burst.
HPROT_M0[3:0]	Input	AHB-Lite protection control for master 0. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M0[1:0]	Output	AHB-Lite transfer response for master 0: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M0[31:0]	Output	AHB-Lite read data for master 0.
HREADY_M0	Output	AHB-Lite ready signal for master 0. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
REMAP_M0	Input	Remap signal for master 0. When this signal is High, slots 0 and 1 are swapped over in the memory space from the viewpoint of master 0.
HADDR_M1[31:0]	Input	AHB-Lite address bus for master 1.
HMASTLOCK_M1	Input	AHB-Lite locked sequence indication for master 1.
HSIZE_M1[2:0]	Input	AHB-Lite transfer size for master 1. Indicates the size of the transfer. Only byte, half-word, and word transactions are supported.
HTRANS_M1[1:0]	Input	AHB-Lite transfer type for master 1. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M1	Input	AHB-Lite write indication for master 1. High for a write, Low for a read.
HWDATA_M1[31:0]	Input	AHB-Lite write data for master 1.

Table 7 • **CoreAHBLite Ports [1]**

Port Name	Type	Description
HBURST_M1[2:0]	Input	AHB-Lite burst type for master 1. Indicates if the transfer forms part of a burst.
HPROT_M1[3:0]	Input	AHB-Lite protection control for master 1. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M1[1:0]	Output	AHB-Lite transfer response for master 1: 00: Okay 01: Error 10: Retry 11: Split HRESP_M1[1] is tied low internally. HRESP_M1[0] = 0 indicates an Okay response and HRESP_M1[0] = 1 indicates an Error response.
HRDATA_M1[31:0]	Output	AHB-Lite read data for master 1.
HREADY_M1	Output	AHB-Lite ready signal for master 1. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
HADDR_M2[31:0]	Input	AHB-Lite address bus for master 2.
HMASTLOCK_M2	Input	AHB-Lite locked sequence indication for master 2.
HSIZE_M2[2:0]	Input	AHB-Lite transfer size for master 2. Indicates the size of the transfer. Only byte, half-word and word transactions are supported.
HTRANS_M2[1:0]	Input	AHB-Lite transfer type for master 2. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M2	Input	AHB-Lite write indication for master 2. High for a write, Low for a read.
HWDATA_M2[31:0]	Input	AHB-Lite write data for master 2.
HBURST_M2[2:0]	Input	AHB-Lite burst type for master 2. Indicates if the transfer forms part of a burst.
HPROT_M2[3:0]	Input	AHB-Lite protection control for master 2. The protection control signals provide additional information on a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M2[1:0]	Output	AHB-Lite transfer response for master 2: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M2[31:0]	Output	AHB-Lite read data for master 2.
HREADY_M2	Output	AHB-Lite ready signal for master 2. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven Low to extend a transfer.
HADDR_M3[31:0]	Input	AHB-Lite address bus for master 3.
HMASTLOCK_M3	Input	AHB-Lite locked sequence indication for master 3.
HSIZE_M3[2:0]	Input	AHB-Lite transfer size for master 3. Indicates the size of the transfer. Only byte, half-word and word transactions are supported.

Table 7 • **CoreAHBLite Ports [1]**

Port Name	Type	Description
HTRANS_M3[1:0]	Input	AHB-Lite transfer type for master 3. Indicates the type of the current transfer: 00: Idle 01: Busy 10: Non-sequential 11: Sequential
HWRITE_M3	Input	AHB-Lite write indication for master 3. High for a write, Low for a read.
HWDATA_M3[31:0]	Input	AHB-Lite write data for master 3.
HBURST_M3[2:0]	Input	AHB-Lite burst type for master 3. Indicates if the transfer forms part of a burst.
HPROT_M3[3:0]	Input	AHB-Lite protection control for master 3. The protection control signals provide additional information about a bus access and are primarily intended for use by a module that wishes to implement some level of protection. These signals are not passed to the slave interface.
HRESP_M3[1:0]	Output	AHB-Lite transfer response for master 3: 00: Okay 01: Error 10: Retry 11: Split HRESP_M0[1] is tied low internally. HRESP_M0[0] = 0 indicates an Okay response and HRESP_M0[0] = 1 indicates an Error response.
HRDATA_M3[31:0]	Output	AHB-Lite read data for master 3.
HREADY_M3	Output	AHB-Lite ready signal for master 3. When asserted, this signal indicates that a transfer has finished on the bus. This signal may be driven low to extend a transfer.
HRDATA_S0[31:0]	Input	AHB-Lite read data from slave 0.
HREADYOUT_S0	Input	AHB-Lite ready signal from slave 0.
HRESP_S0[1:0]	Input	AHB-Lite transfer response from slave 0.
HSEL_S0	Output	AHB-Lite slave 0 select.
HADDR_S0[31:0]	Output	AHB-Lite address bus for slave 0.
HSIZE_S0[2:0]	Output	AHB-Lite transfer size for slave 0.
HTRANS_S0[1:0]	Output	AHB-Lite transfer type for slave 0. HTRANS_S0[0] is tied low internally.
HWRITE_S0	Output	AHB-Lite write indication for slave 0.
HWDATA_S0[31:0]	Output	AHB-Lite write data for slave 0.
HMASTLOCK_S0	Output	AHB-Lite master locked sequence indication for slave 0.
HREADY_S0	Output	AHB-Lite ready signal to slave 0.
HBURST_S0[2:0]	Output	AHB-Lite burst type indication to slave 0. All the transactions towards slave are converted to a single burst irrespective of the value of HBURST_S0.
HPROT_S0[3:0]	Output	AHB-Lite protection control to slave 0.
…	…	…
HRDATA_S15[31:0]	Input	AHB-Lite read data from slave 15.
HREADYOUT_S15	Input	AHB-Lite ready signal from slave 15.
HRESP_S15[1:0]	Input	AHB-Lite transfer response from slave 15.
HSEL_S15	Output	AHB-Lite slave 15 select.
HADDR_S15[31:0]	Output	AHB-Lite address bus for slave 15.
HSIZE_S15[2:0]	Output	AHB-Lite transfer size for slave 15.

Table 7 • **CoreAHBLite Ports [1]**

Port Name	Type	Description
HTRANS_S15[1:0]	Output	AHB-Lite transfer type for slave 15. HTRANS_S15[0] is tied low internally.
HWRITE_S15	Output	AHB-Lite write indication for slave 15.
HWDATA_S15[31:0]	Output	AHB-Lite write data for slave 15.
HMASTLOCK_S15	Output	AHB-Lite master locked sequence indication for slave 15.
HREADY_S15	Output	AHB-Lite ready signal to slave 15.
HBURST_S15[2:0]	Output	AHB-Lite burst type indication to slave 15. All the transactions towards slave are converted to a single burst irrespective of the value of HBURST_S15.
HPROT_S15[3:0]	Output	AHB-Lite protection control to slave 15.
HRDATA_S16[31:0]	Input	AHB-Lite read data from slave 16 (combined region slave or huge slave).
HREADYOUT_S16	Input	AHB-Lite ready signal from slave 16 (combined region slave or huge slave).
HRESP_S16[1:0]	Input	AHB-Lite transfer response from slave 16 (combined region slave or huge slave).
HSEL_S16	Output	AHB-Lite select for slave 16 (combined region slave or huge slave).
HADDR_S16[31:0]	Output	AHB-Lite address bus for slave 16 (combined region slave or huge slave).
HSIZE_S16[2:0]	Output	AHB-Lite transfer size for slave 16 (combined region slave or huge slave).
HTRANS_S16[1:0]	Output	AHB-Lite transfer type for slave 16 (combined region slave or huge slave). HTRANS_S16[0] is tied low internally.
HWRITE_S16	Output	AHB-Lite write indication for slave 16 (combined region slave or huge slave).
HWDATA_S16[31:0]	Output	AHB-Lite write data for slave 16 (combined region slave or huge slave).
HMASTLOCK_S16	Output	AHB-Lite master locked sequence indication for slave 16 (combined region slave or huge slave).
HREADY_S16	Output	AHB-Lite ready signal to slave 16 (combined region slave or huge slave).
HBURST_S16[2:0]	Output	AHB-Lite burst type indication to slave 16 (combined region slave or huge slave). All the transactions towards slave are converted to a single burst irrespective of the value of HBURST_S16.
HPROT_S16[3:0]	Output	AHB-Lite protection control to slave 16 (combined region slave or huge slave).

1. All signals in this table are active high unless otherwise stated.

5 Tool Flows

5.1 Licensing

No license is required to use this core.

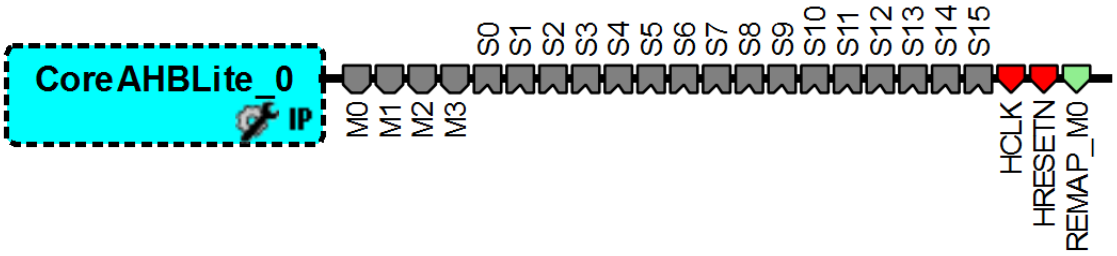
5.1.1 RTL

Complete RTL source code is provided for the core and testbench.

5.2 SmartDesign

CoreAHBLite is available through the Libero SoC IP Catalog. Download it from a remote web-based repository and install into your local vault to make it ready to use. Once installed in the Libero software, you can instantiate, configure, connect, and generate the core using the SmartDesign tool.

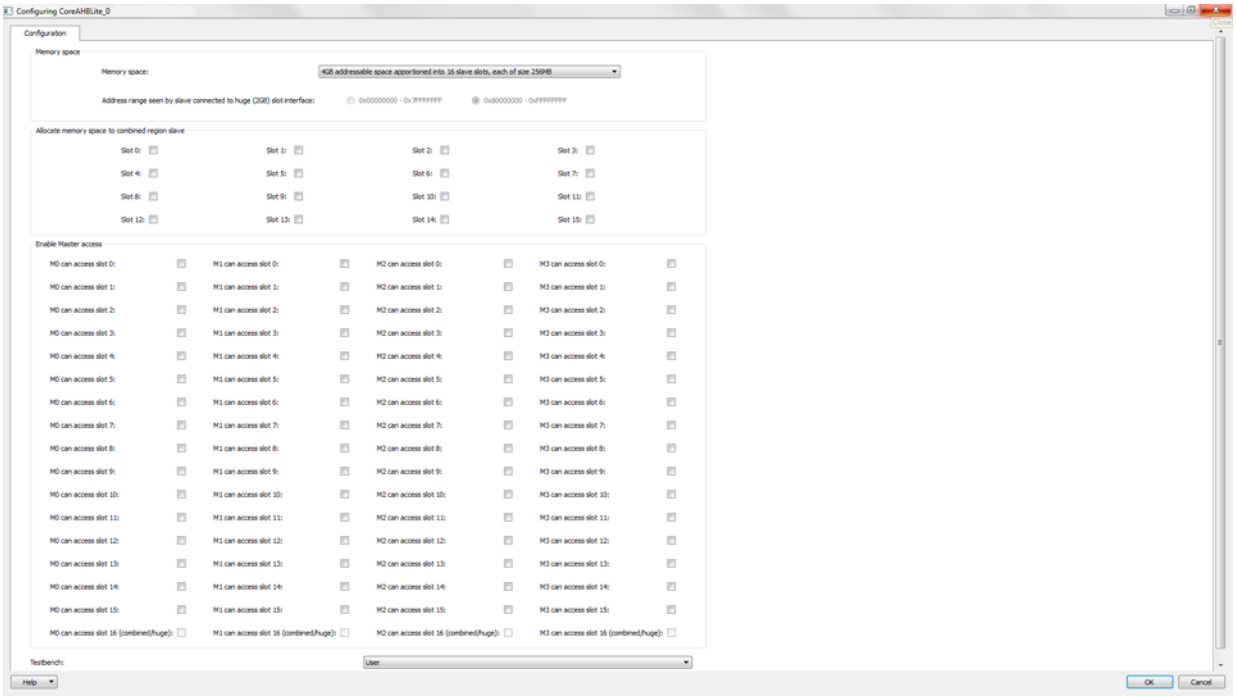
Figure 3 • **SmartDesign CoreAHBLite Instance View**



5.2.1 Configuring CoreAHBLite in SmartDesign

The CoreAHBLite configuration GUI takes up a large amount of screen area when it is sized to show all configuration options. The following figure shows the configuration GUI.

Figure 4 • **CoreAHBLite Configuration GUI**



The configuration options displayed in the configuration GUI correspond with the configuration parameters listed in Table 6, page 8.

For some of the configuration options, tool tips pop up when the mouse pointer hovers over the option in the configuration GUI. These tooltips explain a little more about the related options. The following paragraphs describe the configuration options available for CoreAHBLite with reference to the configuration GUI.

5.2.1.1 Memory Space Configuration

A drop-down list provides seven possible options for the memory space configuration. The first option on the list is "16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000". This setting is typically used in a SmartFusion device. The 16 64 KB slots consume a total address space of 16*64*1024 = 2^{20} bytes and can be addressed using the 20-bit address bus that comes from the SmartFusion MSS to the FPGA fabric. The huge (2 GB) slave is typically used by a fabric based master to access resources in the SmartFusion MSS. Slot 16 is used for the huge slave.

The other options in the drop-down list provide for a memory space that is evenly divided into 16 slots. The total address space consumed by these 16 slots decreases as you descend the list of options. The number of address bits of relevance decreases as the address space reduces.

When the memory space is set to "16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000", a further configuration option is enabled. This option allows you to choose the address range for the huge slave, as seen by the slave connected to the huge slave interface. The huge slave always appears at 0x80000000 - 0xFFFFFFFF from the master's point of view, but the slave itself can be presented with an address range of either 0x00000000 - 0x7FFFFFFF or 0x80000000 - 0xFFFFFFFF. Essentially, this configuration option controls bit 31 of the huge slave address bus.

5.2.1.2 Combining Slave Slots

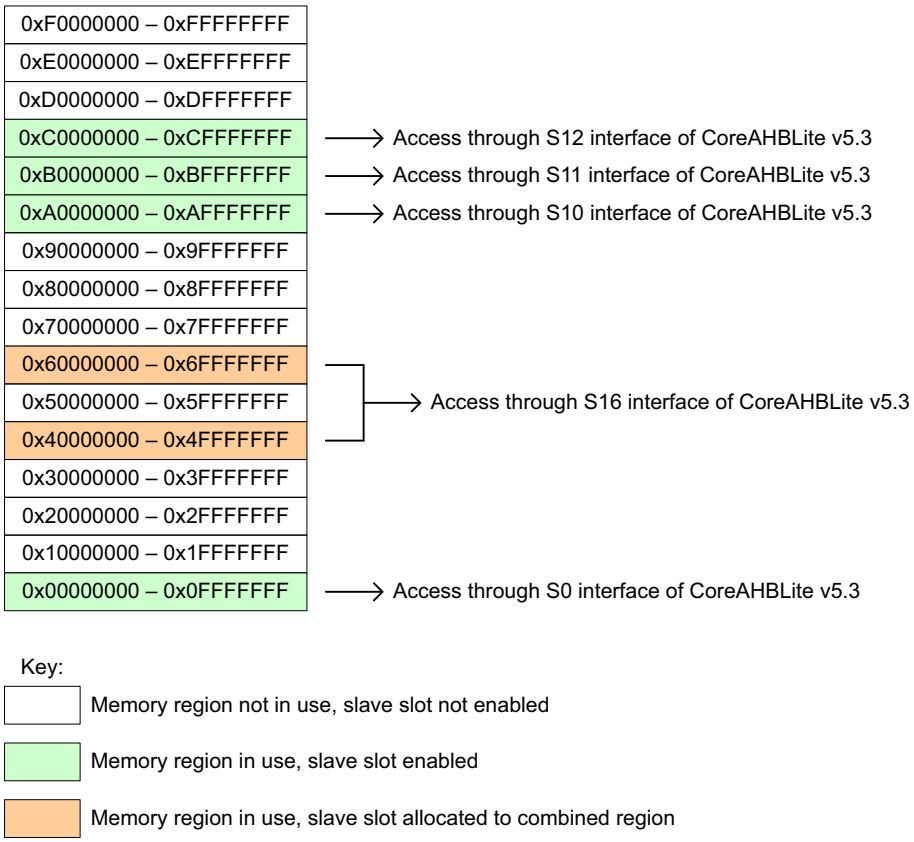
For all memory space configurations, where the total space is evenly divided into 16 slots, one or more slave slots can be assigned to a combined region by selecting the checkboxes in the **Allocate memory space to combined region slave** panel of the configuration GUI.

Note: The slave slot combination is not supported when the memory space is set to "16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000".

When some slots have been allocated to a combined region, an additional slave interface, labeled S16, is displayed for connection on the CoreAHBLite symbol in SmartDesign. Combining slave slots provide a means to access a region larger than the size of a slot through a single slave interface. If slots are combined, they do not necessarily have to be contiguous in the memory space. If a slave slot is allocated to the combined region, then its corresponding interface is no longer available for connection separately.

The following figure shows an example, memory map where slot combining is used. In this example, an AHB-Lite master can access slaves based at addresses 0x00000000, 0xA0000000, 0xB0000000, and 0xC0000000 through individual slave interfaces of CoreAHBLite as shown in Figure 5. Additionally, any access from the master with an address in the ranges 0x40000000 - 0x4FFFFFFF or 0x60000000 - 0x6FFFFFFF results in accessing the S16 slave interface of CoreAHBLite.

Figure 5 • **Example Memory Map Showing Use of Slot Combining**



5.2.1.3 Enabling of Slave Slots

In the **Enable Master access** panel of the configuration GUI, checkboxes are provided to enable or disable access to each slave slot. Access to slave slots can be configured on a per master basis. The enable checkbox for any slot assigned to the combined region is grayed out since it is not possible to connect a slave to such a slot. If a slot is disabled its corresponding interface does not appear for connection on the CoreAHBLite symbol in the SmartDesign tool. The checkboxes for enabling master access to the combined region slave interface (S16) are available to check if some slots are allocated to the combined region.

5.3 Memory Map

There are no addressable resources within CoreAHBLite itself. The core divides the address space seen by a master into a number of slave slots. The following table lists the memory map for CoreAHBLite when the memory space is set to "16 64 KB slots, plus reserved space, plus 1 huge (2 GB) slot beginning at address 0x80000000". For other memory space settings, refer to Table 9, page 18 that shows the allocation of space to each slave slot.

When the memory space is set to other than "16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000", it is possible to combine slots to create a portion of the memory map that can be accessed through an additional combined region slave interface. This interface is labeled S16 on the CoreAHBLite symbol in the SmartDesign tool.

Table 8 • **Memory Map When Memory Space is Set to "16 64 Kb Slots, Reserved Space, and 1 Huge (2 Gb) Slot Beginning at Address 0x80000000[1]**

Resource	Address Space
Slave 0	0x00000000 - 0x0000FFFF
Slave 1	0x00010000 - 0x0001FFFF
Slave 2	0x00020000 - 0x0002FFFF
Slave 3	0x00030000 - 0x0003FFFF
Slave 4	0x00040000 - 0x0004FFFF
Slave 5	0x00050000 - 0x0005FFFF
Slave 6	0x00060000 - 0x0006FFFF
Slave 7	0x00070000 - 0x0007FFFF
Slave 8	0x00080000 - 0x0008FFFF
Slave 9	0x00090000 - 0x0009FFFF
Slave 10	0x000A0000 - 0x000AFFFF
Slave 11	0x000B0000 - 0x000BFFFF
Slave 12	0x000C0000 - 0x000CFFFF
Slave 13	0x000D0000 - 0x000DFFFF
Slave 14	0x000E0000 - 0x000EFFFF
Slave 15	0x000F0000 - 0x000FFFFF
(Reserved)	0x00100000 - 0x7FFFFFFF
Huge slave (Slave 16)	0x80000000 - 0xFFFFFFFF

1. The slave connected to the huge slave interface (S16) can see an address range of either 0x80000000 - 0xFFFFFFFF or 0x00000000 - 0x7FFFFFFF depending on how the core is configured. From the master's point of view, the huge slave always appears in the range 0x80000000 - 0xFFFFFFFF.

Table 9 • **Memory Map for a Range of Memory Space Settings other than "16 64 KB slots, reserved space, and 1 huge (2 GB) slot beginning at address 0x80000000"**

Total address space	**4 GB**	**256 MB**	**…**	**64 KB**	**4 KB**
Resource	**Address Space**				
Slave 0	0x00000000 - 0x0FFFFFFF	0x00000000 - 0x00FFFFFF		0x00000000 - 0x0000FFFF	0x00000000 - 0x00000FFF
Slave 1	0x10000000 - 0x1FFFFFFF	0x01000000 - 0x01FFFFFF		0x00010000 - 0x0001FFFF	0x00001000 - 0x00001FFF
Slave 2	0x20000000 - 0x2FFFFFFF	0x02000000 - 0x02FFFFFF		0x00020000 - 0x0002FFFF	0x00002000 - 0x00002FFF
Slave 3	0x30000000 - 0x3FFFFFFF	0x03000000 - 0x03FFFFFF		0x00030000 - 0x0003FFFF	0x00003000 - 0x00003FFF
Slave 4	0x40000000 - 0x4FFFFFFF	0x04000000 - 0x04FFFFFF		0x00040000 - 0x0004FFFF	0x00004000 - 0x00004FFF
Slave 5	0x50000000 - 0x5FFFFFFF	0x05000000 - 0x05FFFFFF		0x00050000 - 0x0005FFFF	0x00005000 - 0x00005FFF
Slave 6	0x60000000 - 0x6FFFFFFF	0x06000000 - 0x06FFFFFF		0x00060000 - 0x0006FFFF	0x00006000 - 0x00006FFF
Slave 7	0x70000000 - 0x7FFFFFFF	0x07000000 - 0x07FFFFFF		0x00070000 - 0x0007FFFF	0x00007000 - 0x00007FFF
Slave 8	0x80000000 - 0x8FFFFFFF	0x08000000 - 0x08FFFFFF		0x00080000 - 0x0008FFFF	0x00008000 - 0x00008FFF
Slave 9	0x90000000 - 0x9FFFFFFF	0x09000000 - 0x09FFFFFF		0x00090000 - 0x0009FFFF	0x00009000 - 0x00009FFF
Slave 10	0xA0000000 - 0xAFFFFFFF	0x0A000000 - 0x0AFFFFFF		0x000A0000 - 0x000AFFFF	0x0000A000 - 0x0000AFFF
Slave 11	0xB0000000 - 0xBFFFFFFF	0x0B000000 - 0x0BFFFFFF		0x000B0000 - 0x000BFFFF	0x0000B000 - 0x0000BFFF
Slave 12	0xC0000000 - 0xCFFFFFFF	0x0C000000 - 0x0CFFFFFF		0x000C0000 - 0x000CFFFF	0x0000C000 - 0x000CFFF
Slave 13	0xD0000000 - 0xDFFFFFFF	0x0D000000 - 0x0DFFFFFF		0x000D0000 - 0x000DFFFF	0x0000D000 - 0x0000DFFF
Slave 14	0xE0000000 - 0xEFFFFFFF	0x0E000000 - 0x0EFFFFFF		0x000E0000 - 0x000EFFFF	0x0000E000 - 0x0000EFFF
Slave 15	0xF0000000 - 0xFFFFFFFF	0x0F000000 - 0x0FFFFFFF		0x000F0000 - 0x000FFFFF	0x0000F000 - 0x0000FFFF

6 System Integration

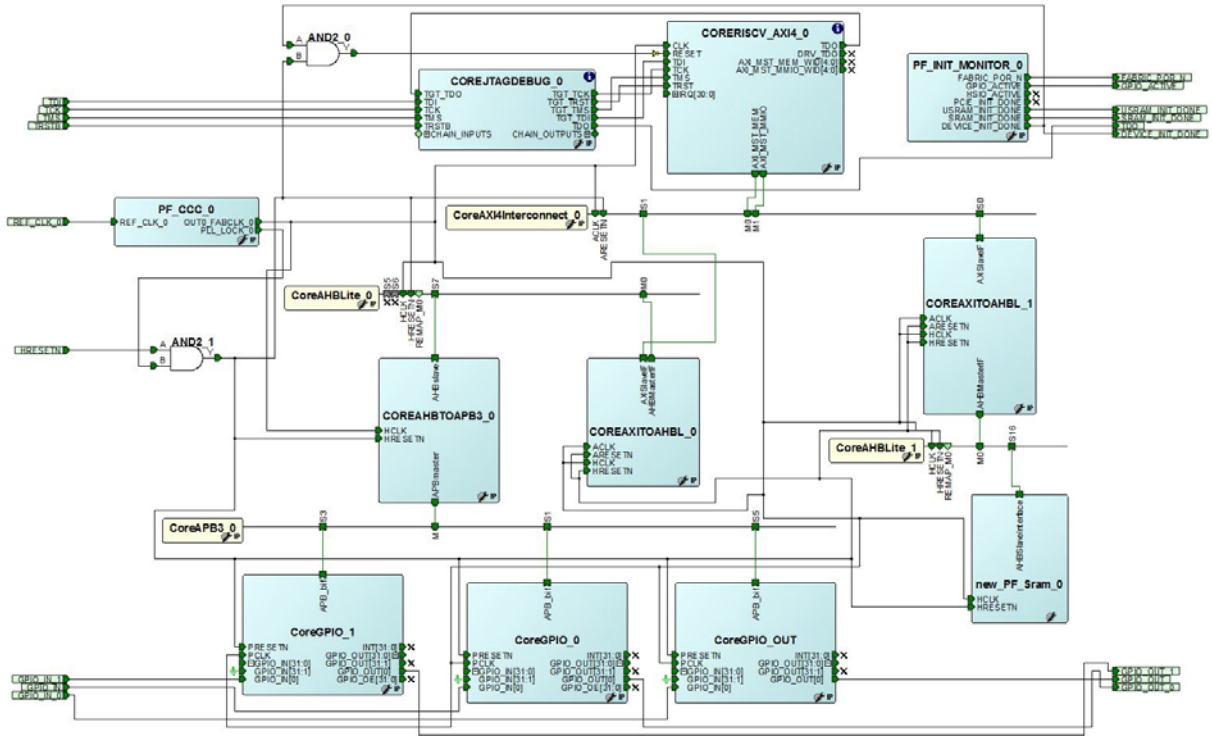
This section provides hints to ease the integration of CoreAHBLite.

The example design tests a simple I/O application for CoreGPIO interfaced with RISCV through CoreAHBLite on PolarFire EVAL KIT.

In the design,

- CoreGPIO_0, CoreGPIO_1, CoreGPIO_OUT are connected to CoreRISCV_AXI4_0 through CoreAXI4Interconnect_0, CoreAXITOAHBL_0, CoreAHBLite_0, COREAHBTOAPB3_0, and COREAPB3_0
- CoreGPIO_0, CoreGPIO_1, CoreGPIO_OUT are configured by CoreRISCV_AXI4_0 firmware.

Figure 6 • **CoreAHBLite Example Design**



- HRESETN which is and with PF_CCC_0/PLL_LOCK_0 is used for all the resets.
- 50MHz on-board oscillator provides the input clock for PF_CCC_0.
- CoreAHBLite_0 has PCLK driven from PF_CCC_0/OUT0_FABCLK_0.
- CoreGPIO_0 is configured with 8bit of APB_WIDTH, CoreGPIO_1 with 16bit APB_WIDTH and CoreGPIO_OUT with 32 bit APBWIDTH.
- GPIO_OUT, GPIO_OUT_0, GPIO_OUT_1 output ports are connected to LEDs.
- GPIO_IN, GPIO_IN_0, GPIO_IN_1 input ports are connected to switches on the board.
- CoreRISCV_AXI4 firmware configures the instances of CoreGPIO through CoreAXI4Interconnect_0, CoreAXITOAHBL_0, CoreAHBLite_0, COREAHBTOAPB3_0, and COREAPB3_0.
- The firmware checks for CoreGPIOs' input status and accordingly writes onto CoreGPIOs' output ports.