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Release Notes
CoreAHBL2AHBL_Bridge v2.0

Microsemi
Power Matters.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 CoreAHBL2AHBL_Bridge v2.0 Release Notes

These release notes accompany the production release of CoreAHBL2AHBL_Bridge v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Features

CoreAHBL2AHBL_Bridge has the following features:

- Two different asynchronous clock domains for the master and slave interfaces
- Two clocks can be from different clock sources with any type of ratio, for example, integer or fractional multiplier
- Single read, single write transactions
- Burst Mode—INCR, INCR4, INCR8, INCR16 with busy transfer type
- Extended HREADY

2.2 Delivery Types

CoreAHBL2AHBL_Bridge does not require a license to be used and instantiated. The complete RTL source code is available for the core

2.3 Supported Families

PolarFire™

2.4 Supported Tool Flows

CoreAHBL2AHBL_Bridge requires Libero® System-on-Chip (SoC) software v12.0 or later.

2.5 Installation Instructions

The CoreAHBL2AHBL_Bridge CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.6 Documentation

This release contains a copy of the *CoreAHBL2AHBL_Bridge Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.7 Supported Test Environments

Verilog user test bench

2.8 Resolved History

This is the initial version of the CoreAHBL2AHBL_Bridge. There are no unresolved issues in this release.

2.9 Discontinued Features and Devices

This is the initial revision of the core. There are no discontinued features in this release.

2.10 Known Limitations and Workarounds

Wrapping burst is not supported by the IP.