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## CoreABC v3.3 Release Notes

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CoreABC (ABC = APB bus controller) is a simple, configurable, low gate count, programmable controller for use in Advanced Microcontroller Bus Architecture (AMBA) Advanced Peripheral Bus (APB) based designs. CoreABC is an AMBA3 APB master which can connect to and manage APB slave peripherals via an AMBA3 APB bus fabric component such as CoreAPB3.

CoreABC supports a comprehensive assembler based configurable instruction set architecture and extensive and flexible configuration of size and feature options, allowing it to be tuned to meet the resource constraints and processing power requirements of a wide variety of applications.

This is the production release for CoreABC. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

### Features

CoreABC supports the following:

- Extensive configurability, allowing very low cost and resource-efficient implementations
- Programmable APB bus controller
- Hard, soft (RAM), or NVM instruction storage on Actel Fusion<sup>®</sup> devices; hard or soft instruction storage on other device families
- Automatic detection of CoreAI in CoreABC's APB address space and auto-creation of analog configuration MUX (ACM) data, based on CoreAI configuration
- 8-, 16-, and 32-bit APB interface
- In NVM mode, APB data type read and write access to the instruction store memory (via an APB slave interface)
- Built in general purpose input/output (GPIO) signals
- Interrupt-driven operation using interrupt request and interrupt active signals

### Interfaces

CoreABC has an Advanced Microcontroller Bus Architecture (AMBA3) APB master interface that typically will be connected to CoreAPB3.

In NVM mode, an AMBA3 APB slave interface can be used to provide data type access to the instruction store.

In Soft mode, an initialization and configuration (InitCfg) interface is available for initializing the instruction store that contains RAM blocks.

### Delivery Types

CoreABC is licensed as obfuscated or RTL.

#### Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.

Simulation, Synthesis, and Layout can be performed with Actel Libero<sup>®</sup> Integrated Design Environment (IDE). The RTL code for the core is obfuscated.

## RTL

Complete RTL source code is provided for the core and testbenches.

## Supported Families

- IGLOO<sup>®</sup>, IGLOOe, IGLOO PLUS
- ProASIC<sup>®</sup>3, ProASIC3E, ProASIC3L
- SmartFusion<sup>™</sup>
- Fusion
- ProASIC<sup>PLUS</sup><sup>®</sup>
- Axcelerator<sup>®</sup>
- RTAX-S

## Supported Tool Flows

Use Libero IDE v9.0 or later with CoreABC v3.3. Verilog users must use Synopsys<sup>®</sup> Synplify<sup>®</sup> AE v8.2.1 or later. Download the latest software version from [www.synplicity.com](http://www.synplicity.com).

## Installation Instructions

CoreABC is available through the Libero IDE IP Catalog. It can be downloaded from a remote web-based repository and installed into the user's local vault, ready for use. Once installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

## Documentation

This release contains an updated copy of the *CoreABC Handbook*. The handbook can be viewed by right-clicking on the core in the Catalog and selecting **Open documentation > CoreABC\_HB.pdf**. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, place-and-route, and program this core. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at [www.actel.com](http://www.actel.com).

## Supported Test Environments

Verilog and VHDL user testbenches are packaged with the core.

## Discontinued Features and Devices

There are no discontinued features or supported devices.

## New Features and Devices

The following features have been added:

- The use of multiple CoreABC instances in a VHDL based design flow is now correctly supported. Previously, errors would be reported when attempting to generate a SmartDesign design containing multiple instances of CoreABC.
- Support for the SmartFusion family of devices has been added.
- Some improvements have been made to the CoreABC configuration GUI. For example, real time syntax checking when entering a program has been speeded up.

## Resolved Issues in the v3.3 Release

Table 1 lists the Software Action Requests (SARs) that were resolved in the v3.3 release of CoreABC.

Table 1 • Resolved Issues in the CoreABC v3.1 Release

SAR	Description
22474	Configurator Analysis view does not always report the correct maximum program counter value.
29113	Errors with multiple instances of CoreABC in a VHDL design flow
29600	Add explicit support for SmartFusion family.

## Resolved Issues in the v3.1 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the v3.1 release of CoreABC.

Table 2 • Resolved Issues in the CoreABC v3.1 Release

SAR	Description
25193	Compilation of NVM mode CoreABC design fails for AFS090 device.

## Resolved Issues in the v3.0 Release

Table 3 lists the SARs that were resolved in the v3.0 release of CoreABC.

Table 3 • Resolved Issues in the CoreABC v3.0 Release

SAR	Description
21840 11788	Some instruction sequences result in erroneous behavior due to a multiplexer select bit not being properly controlled.
11789	Memory files not generated correctly in Soft mode.
11574	ACM lookup table data incorrect/incomplete for certain CoreAI configurations.
11597	Incorrect library mappings in the debugblk.vhd file causes problems in the obfuscated VHDL flow.
12014	Initialization and configuration (InitCfg) interface not grouped as bus interface.
23069	Instruction skipped when returning from active Low interrupt.
23356	Failing conditional checks based on general purpose inputs 10, 18, and 27.

## Resolved Issues in the v2.3 Release

Table 4 lists the SARs that were resolved in the v2.3 release of CoreABC.

Table 4 • Resolved Issues in the CoreABC v2.3 Release

SAR	Description
63779	Instruction enhancements have been made to support the following: <ul style="list-style-type: none"> <li>• ALU operations on RAM contents</li> <li>• Indirect APB addressing</li> <li>• IOWRT and IOREAD enhancements</li> <li>• Multiply support</li> </ul>
61286	The Analysis window calculates the INITWIDTH value from the number of instructions in use rather than the configured ICWIDTH parameter.

**Table 4 • Resolved Issues in the CoreABC v2.3 Release (continued)**

63977 63697	Pressing the ESC key in the assembler exits the assembler without saving edits. The GUI now opens a confirmation window before exiting when changes have been made.
64835	CoreABC firmware is lost if analyze is used instead of saving it.
64031	Configuration GUI incorrectly gives an error when the loop counter (Z register) is disabled.
64585	When using the numeric keypad, double digits are entered.
64586	Cannot use "DEF ADDRESS 0" in the configurator.
64588	Analysis does not check if instructions are enabled. This information is shown in the Parameters window. The Parameters window must be checked prior to exiting the Configurator to verify that only enabled instructions have been used.
65657	The Assembler/Configurator allows saving inconsistent configurations and programs. Users must verify that no warnings are shown in both the Parameters and Program windows of the Configurator before exiting the Configurator.

## Resolved Issues in the v2.2 Release

CoreABC v2.2 was not released. [Table 5](#) lists the SARs that were resolved in v2.2 of CoreABC.

**Table 5 • Resolved Issues in CoreABC v2.2 Release**

SAR	Description
63778	APB access to slots $\geq 2$ . When accessing slots 2, 6, 8, etc., CoreABC would actually access APB slot 0. When addressing slots 3, 5, 7, 9, etc., the core would actually address slot 1. This has been corrected. The core now correctly accesses the appropriate APB slot.
64208	RETURN clears INTACT. The RETURN instruction clears the internal interrupt active bit and the INTACT output. Only the RETISR instruction should have cleared this bit.

## Resolved Issues in the v2.1 Release

The v2.1 release contains an updated handbook. No changes have been made to the RTL code apart from updating version numbers in the source files.

## Resolved Issues in the v2.02 Release

This was the first core production release; hence there are no resolved issues from a previous release.

## Known Issues in the v3.3 Release

[Table 6](#) lists the known issues in v3.3 release of CoreABC.

**Table 6 • Known Issues in the CoreABC v3.3 Release**

SAR	Description
11513	Assembler does not support operations on immediate values. For example, an instruction such as "RAMWRT DAT \$VALUE+7" cannot be used because the "\$VALUE+7" expression is not supported.



**Microsemi Corporate Headquarters**  
2381 Morse Avenue, Irvine, CA 92614  
Phone: 949-221-7100 · Fax: 949-756-0308  
[www.microsemi.com](http://www.microsemi.com)

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